OPERATING AND SERVICE MANUAL

TIMER/COUNTER

5304A

HEWLETT hp PACKARD

CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

WARRANTY AND ASSISTANCE

This Hewlett-Packard product is warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard. No other warranty is expressed or implied. We are not liable for consequential damages.

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MODEL NUMBER:

5304A TIMER/COUNTER

HEWLETT-PACKARD WELCOMES YOUR EVALUATION OF THIS MANUAL. CHECK THE APPROPRIATE BOXES, AND LIST ANY COMMENTS YOU MAY HAVE.

	SECTION	I	II	III	IV	V	VI	VII	VIII
1. DOES EACH SECTION CONTAIN THE INFORMATION YOU NEED?	YES	☐	☐	☐	☐	☐	☐	☐	☐
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	NO	☐	☐	☐	☐	☐	☐	☐	☐
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- SPECIFICATIONS ☐
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SECTION IX D
TIMER/COUNTER
5304A

SERIAL PREFIX: 1212A00467

This section applies directly to HP Model 5304A, Timer/Counters having serial prefix number 1212A00467, and must be inserted into the 5300A Measuring System Manual.

NEWER INSTRUMENTS

This Section with enclosed "Manual Changes Pages" applies directly to HP Model 5304A Timer/Counters having prefix numbers above 1212A00467.

OLDER INSTRUMENTS

Changes required to back-date this Section for older instruments are in Section IX D, Subsection VII.

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HP PART NO.
MANUAL 05304-90006

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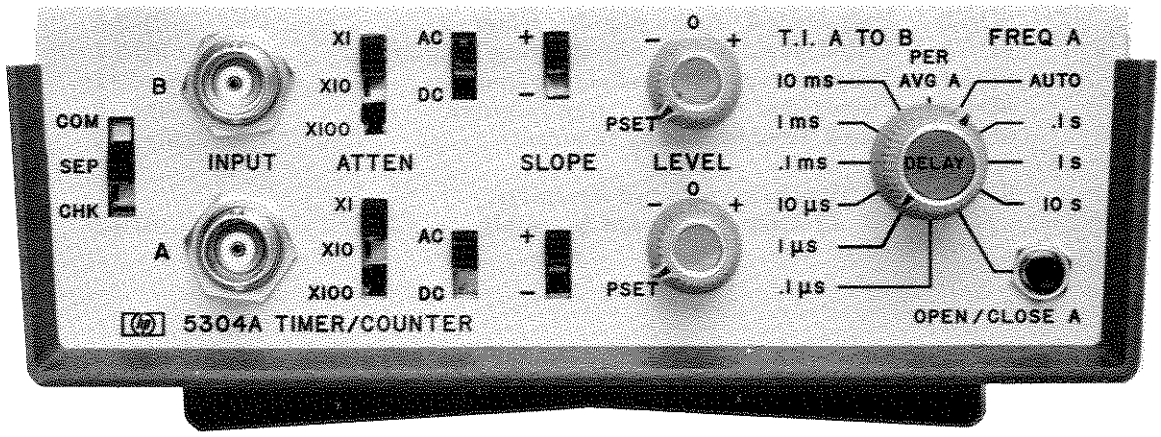
TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Figure 9D-1-1. 5304A Timer/Counter



SECTION IX D
5304A TIMER/COUNTER

SUBSECTION I
GENERAL INFORMATION

9D-1-1. INTRODUCTION

9D-1-2. Description

9D-1-3. The Hewlett-Packard Model 5304A/Timer Counter, when plugged onto an HP Model 5300A Measuring System, is capable of: Measuring frequencies up to 10 MHz, Time Interval measurements from 500 nsec to 10,000 seconds, Period Average over a range of 10 Hz to 1 MHz, and Totalizing. The electrical and mechanical specifications are listed in Table 9D-1-1.

9D-1-4. Purpose and Use of Section IX D

9D-1-5. Section IX D contains the documentation necessary to operate, maintain, and repair the HP Model 5304A Timer/Counter plug-on. Also included are parts lists, component locators, and schematics. This information is intended to be inserted into the 5300A Measuring System manual as part of Section IX of that manual.

9D-1-6. INSTRUMENT IDENTIFICATION

9D-1-7. Hewlett-Packard uses a two-section, nine-digit serial number (0000A00000) mounted on the rear panel to identify the instrument. The first four digits are the serial prefix and the last five digits refer to the specific instrument. If the serial prefix on your instrument differs from that listed on the title page of this section, there are differences between the manual and your instrument. Lower serial prefixes are documented in Section IX D, Subsection VII and higher serial prefixes are covered by a manual change sheet included with the manual.

9D-1-8. Manual Changes and Options

9D-1-9. The title page lists the serial prefix number to which this information directly applies. If the serial prefix is different from the one listed, a change sheet is included describing the required changes. If this change sheet is missing, the information can be supplied by any Hewlett-Packard Sales and Service office listed in Section VI of the 5300A Measuring System Manual. Options are listed in Section IX D, Subsection VII.

Table 9D-1-1. 5304A Timer/Counter Specifications

INPUT CHANNELS A AND B

Range: DC coupled; 0 to 10 MHz.
AC coupled; 100 Hz to 10 MHz.

Sensitivity (min): 25 mV rms sine wave to 1 MHz. 50 mV rms sine wave to 10 MHz. 150 mV p-p pulse at minimum pulse width, 40 nsec. Sensitivity can be decreased by 10 or 100 times using ATTENUATOR switch.

Impedance: 1 MΩ shunted by less than 30 pF.

Overload Protection: 250 V rms on X10 and X100 attenuator settings. On X1 attenuator setting 120 V rms up to 1 kHz, decreasing to 10 V rms at 10 MHz.

Trigger Level: PRESET position centers triggering about 0 volts ±25 mV, or continuously variable over the range of -1 V to +1 V times attenuator settings.

Slope: Independent selection of triggering on positive or negative slope.

Channel Inputs: Common or separate lines.

Gate Output: Rear panel BNC. TTL low level while gate is open. May be used to intensity modulate an HP oscilloscope.

TIME INTERVAL

Range: 500 nsec to 10^4 sec.

Input: Channels A and B; can be common or separate.

Overload: Maximum recommended levels for pulse signals is 2 V p-p. Clipping occurs at 3 V p-p.

Resolution: 100 nsec to 10 ms in decade steps.

Accuracy: ±1 count ± time base accuracy ± trigger error.*

Display: μs, ms, or s (seconds) with positioned decimal point.

Time Interval Holdoff: Front panel concentric knob which inserts variable delay of approximately 100 μsec to 100 msec between START (Channel A) and enabling STOP (Channel B); may be disabled. Electrical inputs during delay time are ignored. Delay may be digitally measured in CHECK position. Delay Output: rear panel BNC. TTL low level during delay time. May be used to intensity modulate an HP oscilloscope.

PERIOD AVERAGE

Range: 10 Hz to 1 MHz.

Input: Channel A.

Period Averaged: 1 to 10^3 automatically selected for maximum resolution.

Frequency Counted: 10 MHz.

Accuracy: ±1 count ± time base accuracy ± trigger error.**

Display: μs, ms with positioned decimal point.

FREQUENCY

Range: 0 to 10 MHz.

Input: Channel A.

Gate Times: Manually selected 0.1, 1, or 10 seconds. AUTO position selects gate time to fill display for maximum resolution within a 1-second measurement time.

Accuracy: ±1 count ± time base accuracy.

Display: Hz, kHz, and MHz with positioned decimal point.

OPEN/CLOSE (Totalizing)

Range: 10 MHz maximum.

Input: Channel A.

Function: Input signal totalized while gate open. Opening and closing of gate initiated by front panel pushbutton switch.

GENERAL

Check: Inserts internal 10 MHz reference frequency into Channels A and B. Time Interval Holdoff may be digitally measured by switching to CHECK and TIME INTERVAL positions.

Operating Temperature: 0° to 50°C.

Power Requirements: Including 5300A mainframe, nominally 10 watts. Minimum of 3 hours operation (typically 5 hrs) at 20°C to 30°C operating and charging temperatures.

Weight: Net, 1 lb (0.9 kg). Shipping, 3¼ lbs (1.5 kg).

*For any waveshape, trigger error is less than

$$\pm \frac{0.005}{\text{Signal Slope (V/ } \mu\text{s)}} \mu\text{s}$$

**Trigger error is less than ±0.3% of one period. ÷ periods averaged for signal with 40 dB or better signal-to-noise ratio.

SECTION IX D
5304A TIMER/COUNTER

SUBSECTION II
INSTALLATION

9D-2-1. UNPACKING AND INSPECTION

9D-2-2. If the shipping carton is damaged ask that the carrier's agent be present when the instrument is unpacked. Inspect the instruments for damage such as scratches, dents, broken knobs, etc. If the instrument is damaged or fails to meet performance tests when used with the 5300A Measuring System notify the carrier and the nearest Hewlett-Packard Sales and Service office immediately. Performance check procedures are located in Section IX D-5, and Sales and Service offices are listed in Section VI of the 5300A portion of the manual. Retain the shipping carton and the padding material for the carrier's inspection. The Sales and Service office will arrange for the repair or replacement of the instrument without waiting for the claim against the carrier to be settled.

9D-2-3. STORAGE AND SHIPMENT

9D-2-4. PACKAGING. To protect valuable electronic equipment during storage or shipment always use the best packaging methods available. Your Hewlett-Packard Sales and Service office can provide packaging material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable customer packaging on short notice. Here is one recommended packaging method:

a. The original container is a corrugated cardboard box with 200 lbs. burst test (HP No. 9211-1620). The instrument is secured and protected, while in the box by a top and bottom molded form of polystyrene foam (HP No. 9220-1545). Also included with the instrument is a plastic dust-protection cover HP Part No. 05300-80004.

9D-2-5. INSTALLATION AND REMOVAL OF PLUG-ON

9D-2-6. The 5304A Timer/Counter must be used with a mating 5300A Measuring System before any measurements can be made. To mate the 5304A Timer/Counter with the 5300A Measuring System, see Figure 2-1 and Paragraph 2-1 of the 5300A portion of the manual.

9D-2-7. ENVIRONMENT. Conditions during storage and shipment should be normally limited as follows:

a. Maximum altitude: 25,000 feet

b. Minimum temperature: -40°F (-40°C).

c. Maximum temperature: +167°F (+75°C).

9D-2-8. PORTABLE OPERATION

9D-2-9. The use of the HP Model 5310A Battery Pack enables the 5300A Measuring System and 5304A Timer/Counter to be used in areas removed from ac power sources. The 5310A Battery Pack provides a minimum of 3 hours operation (typically 5 hours) at 20°C to 30°C operating and charging temperature. Tables 1-2 and 1-4 of 5300A portion of the manual list the HP 5310A Battery Pack as an available accessory. Documentation on the 5310A is also included in Section IV through VIII of the 5300A portion of the manual. To prepare the 5300A/5304A for portable operation, refer to Paragraph 2-15 and Figure 2-2, steps a to c of 5300A portion of manual.

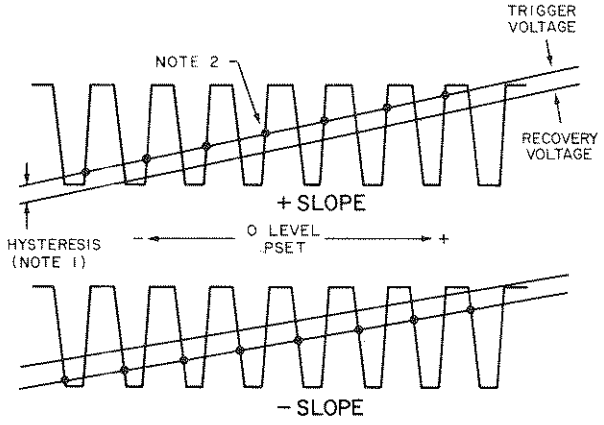
SECTION IX D
5304A TIMER/COUNTER

SUBSECTION III
OPERATION

9D-3-1. OPERATING INFORMATION

9D-3-2. The 5300A/5304A Timer/Counter measures frequencies up to 10 MHz, period average to 1 MHz, time interval from 500 nsec to 10,000 seconds; or totalizes input signals.

Figure 9D-3-1. Signal Conditioning Using Attenuator, Level and Slope Controls



1. HYSTERESIS (NOISE REJECTION) VOLTAGE IS CONSTANT FOR EACH ATTENUATOR SETTING AND DOES NOT VARY WITH TRIGGER LEVEL.
2. THIS ALLOWS ZERO VOLTS TRIGGERING WITH GOOD NOISE REJECTION
3. ATTENUATOR: X1, X10, X100 CHANGES TRIGGER LEVEL AND HYSTERESIS VOLTAGES BY FACTORS OF 1, 10, 100

9D-3-3. There are four basic signal conditioning controls used in Channel A or Channel B (the effect of these controls is shown in Figure 9D-3-1). These are:

a. ATTEN switches for Channel A and B.

b. SLOPE switches for Channel A and B.

c. LEVEL controls for Channel A and B.

d. AC-DC switches for Channel A and B.

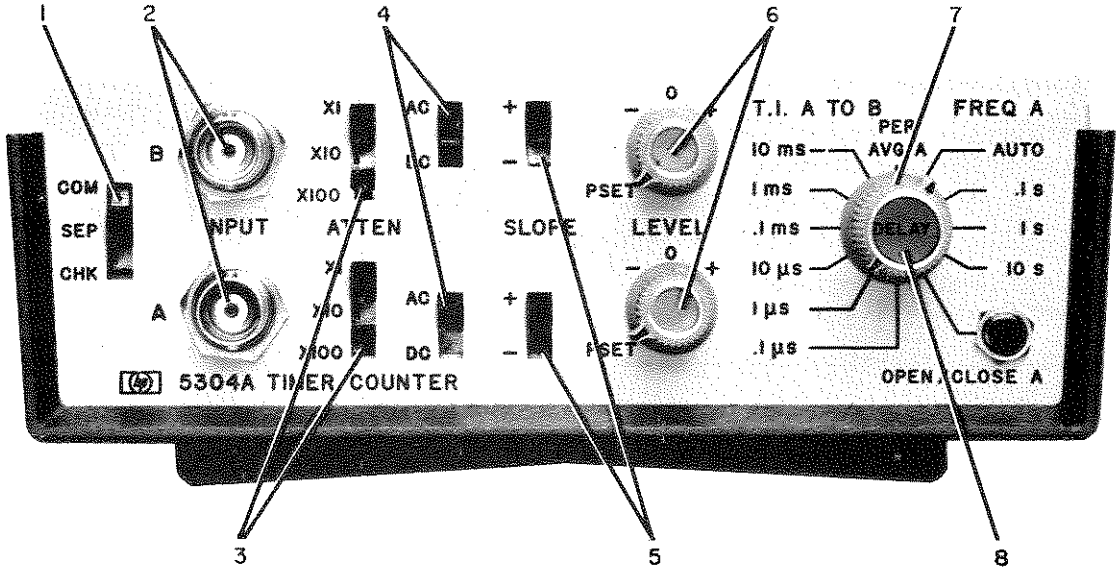
9D-3-4. ATTEN. X1, X10, X100 switches (both Channels. Large amplitude signals can be attenuated by using the ATTEN switches. Setting the attenuator switches increases the trigger levels and the hysteresis voltages by factors of 1, 10, 100. If input signal levels are unknown, the initial measurements should be made with the attenuator switches set to X100. The attenuator settings are then reduced until a stable, useable measurement is obtained.

9D-3-5. SLOPE Switches (both Channels). The slope switches allow the selection of triggering on the positive (+) or negative (-) slope of the input signals (see Figure 9D-3-1).

9D-3-6. LEVEL Controls (both Channels). The level controls allow adjustment of the triggering point on the input signal waveform. With the LEVEL controls set to PSET or "0", triggering is centered about zero volts. The voltage range over which triggering may be set is -1 volt to +1 volt times the ATTEN switch settings (±1 V to ±100 V).

9D-3-7. AC-DC Switches (both Channels). The AC-DC switches select ac or dc coupling. In AC position and PSET, triggering is centered about ac-zero, and dc components on the signal have no effect. In DC position and PSET, triggering is centered about 0 volts dc on the signal.

Figure 9D-3-2. Front-Panel Controls and Connectors



1. COM-SEP-CHK. Three position switch enables selection of input signal from separate or common sources or enables the selection of a Self-Check position.
   a. COM: Connects INPUT A and INPUT B in parallel.
   b. SEP: Channel A and Channel B inputs are from separate sources.
   c. CHK: Self-Check verifies that 5300A 10 MHz crystal oscillator and counting logic and the 5304A gating logic is functioning correctly.
2. INPUT A and B. Input signal frequencies to be measured are connected to INPUT A. INPUT B is used in time interval measurements.
3. ATTEN. Three-position input signal attenuator for both channels.
   a. X1: Connects input signals directly to input amplifiers.
   b. X10: Attenuates input signals by factor of 10.
   c. X100: Attenuates input signals by factor of 100.

Figure 9D-3-2. Front-Panel Controls and Connectors (Continued)

4. AC-DC. Two-position switch allows selection of ac-coupling or direct-coupling to input amplifiers.

5. SLOPE +, -. Selects the triggering on positive or negative slope of the input signals.

6. LEVEL. Adjusts the input trigger levels. Preset to trigger at 0 volts.

7. FUNCTION. Twelve-position switch enables 4 modes of operations to be selected. The modes are:

   a. T.I. A to B: Enables time interval measurements to be made from 500 nsec to 10,000 seconds. Resolution is adjustable from .1 μs to 10 ms in six decade steps.

   b. PER AVG A: Enables multiple period averages to be made from Channel A with frequencies of 10 Hz to 1 MHz. Periods averaged are automatically selected from 1 to 10^3.

   c. FREQ A: Enables frequency measurements from 0 to 10 MHz when dc coupled and 100 Hz to 10 MHz when ac coupled.

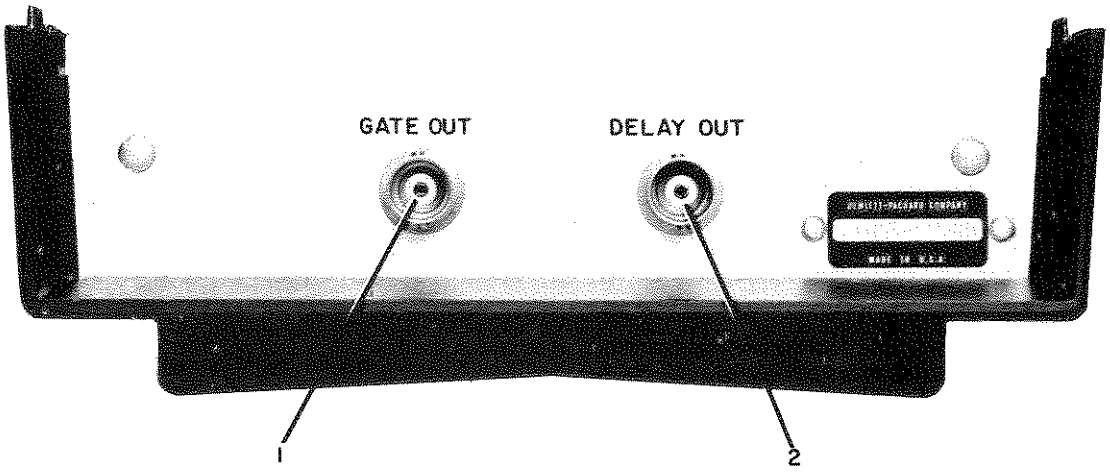
   1) AUTO: Gate time is automatically selected to fill the display for maximum resolution of the signal being measured, without overflow, up to a maximum of 1 second.

   2) .1S, 1S, 10S: Counter gate time is manually selected for .1 second, 1 second or 10 seconds.

   d. OPEN/CLOSE A (Totalize): Enables input signals to Channel A to be totalized. Totalizing is initiated by pressing OPEN/CLOSE A switch and terminated by pressing the switch a second time.

8. DELAY. Adjustment inserts a time interval delay of 100 μsec to 100 msec between Start (Channel A) signal and Stop (Channel B) signal; when disabled, there is a residual delay of about 200 nsec.

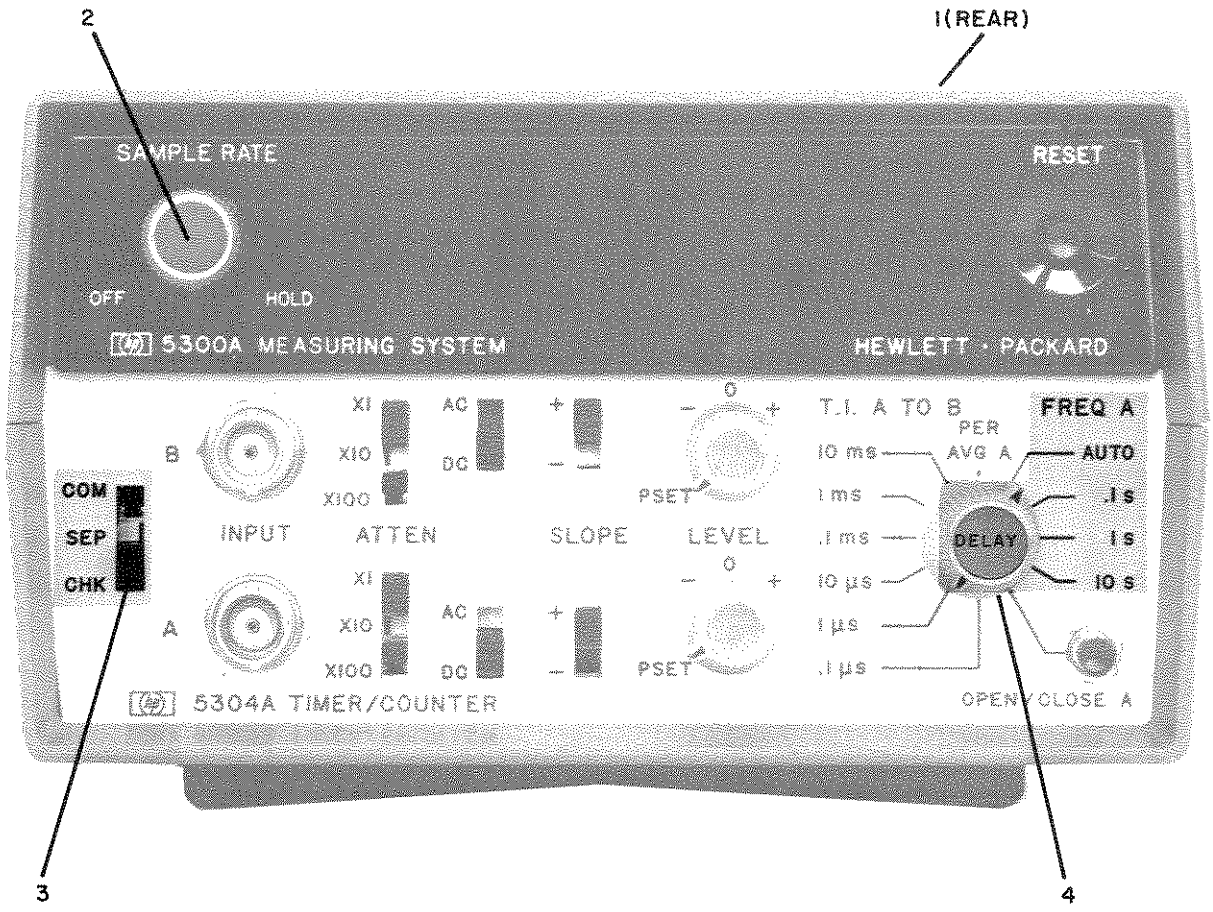
Figure 9D-3-3. Rear-Panel Connectors



1. GATE OUT: A TTL-LOW level signal while the 5300A main gate is open.

2. DELAY OUT: A TTL-LOW level signal during the delay time selected by front-panel DELAY control (in T.I. A to B mode only).

Figure 9D-3-4. Making Self-Check Measurements



1. Connect ac power to 5300A ac receptacle.

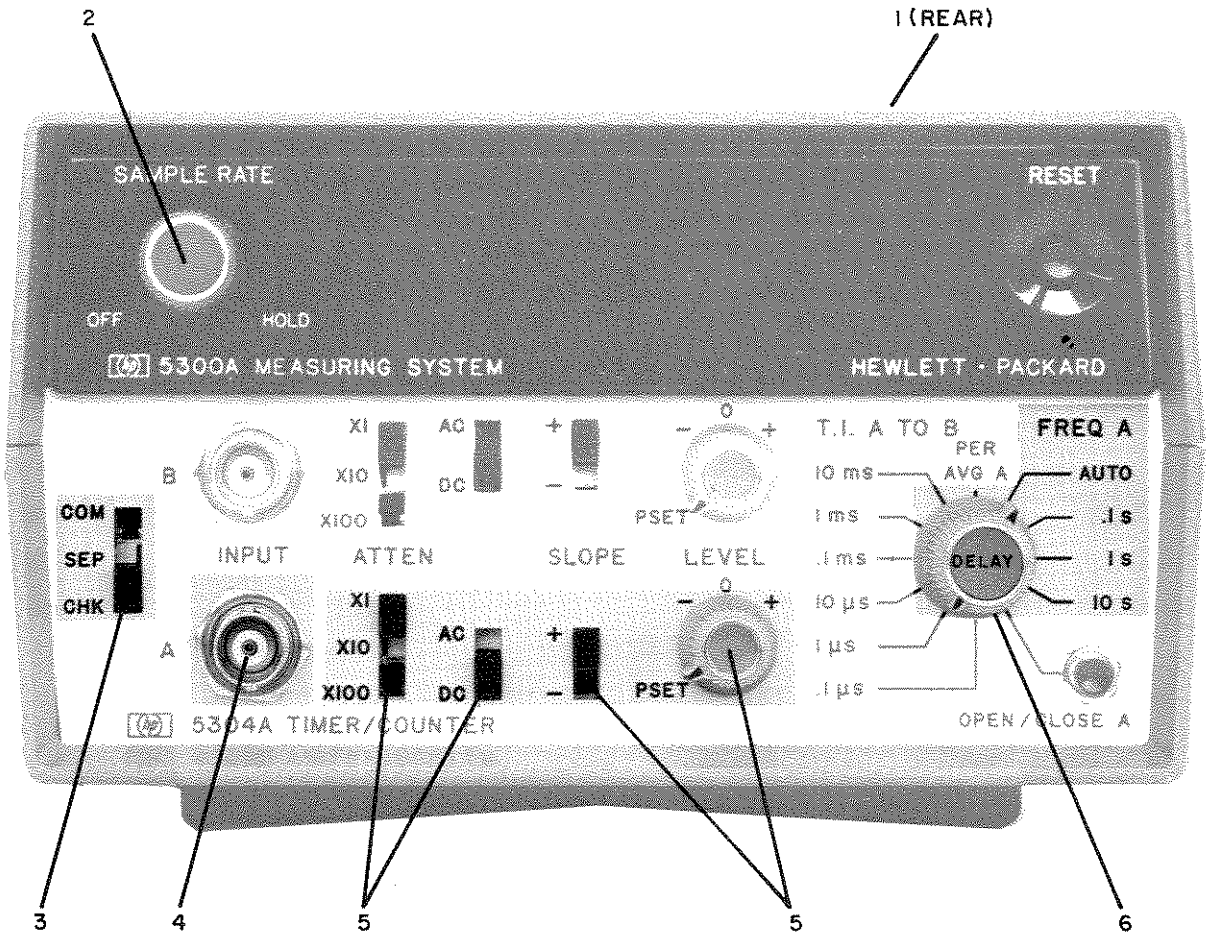
2. Turn ac power "on" with 5300A SAMPLE RATE control. Adjust SAMPLE RATE for desired display time.

3. Set 5304A COM-SEP-CHK switch to CHK.

4. Set 5304A "Function" switch to FREQ A, AUTO. Display should be 10.0000 MHz, ±1 count.

5. The time interval hold-off may be measured by selecting on of the T.I. A to B positions of the "Function" switch.

Figure 9D-3-5. Making Frequency A Measurements



1. Connect ac power to 5300A ac receptacle.

2. Turn ac power "on" with 5300A SAMPLE RATE control and adjust sample rate for desired display time.

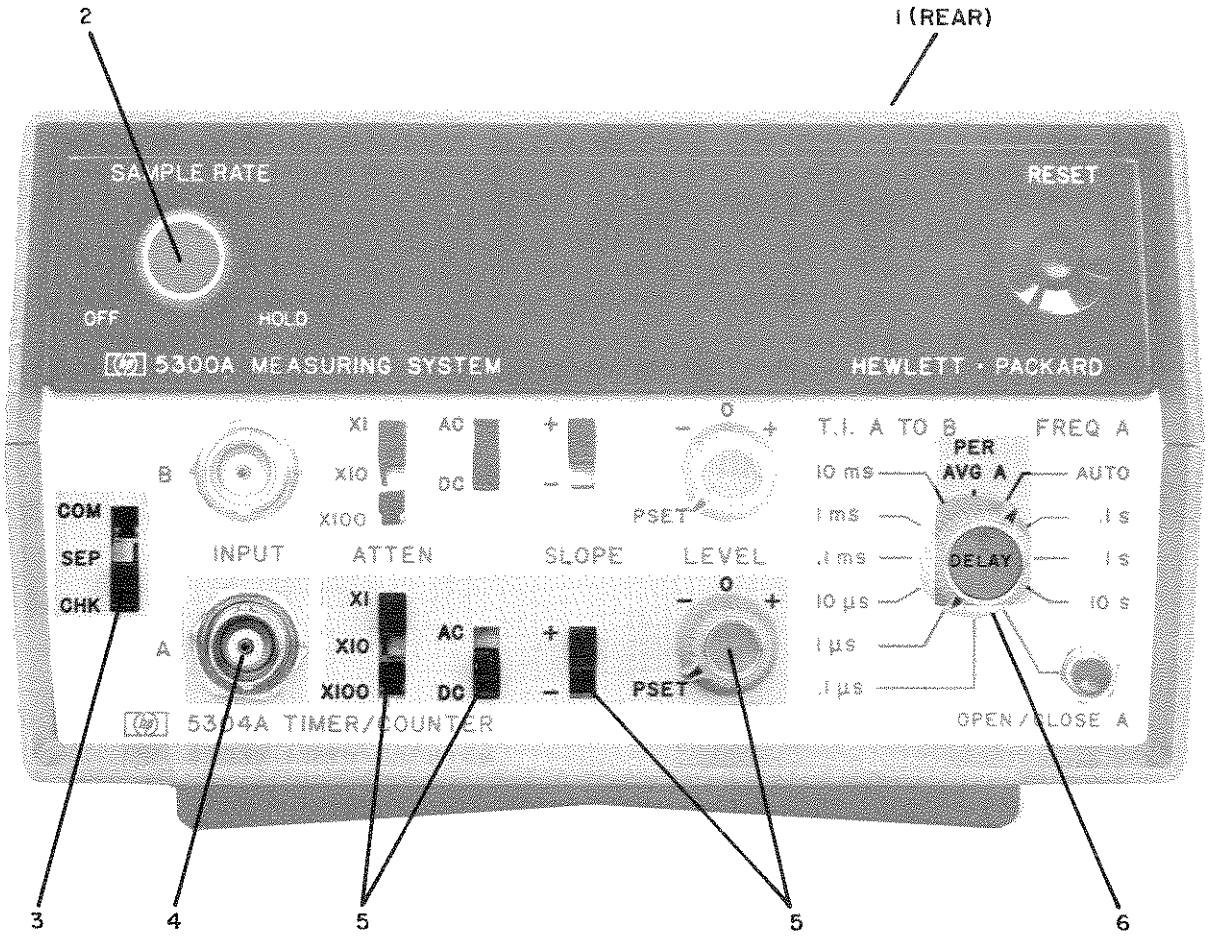
3. Set COM-SEP-CHK to SEP.

4. Connect input signal to INPUT A jack.

5. Set ATTEN to X100; AC-DC to coupling desired and SLOPE to polarity desired. Set LEVEL to PSET.

6. Set "Function" to FREQ A, AUTO and adjust the ATTEN switch until a stable display is obtained. The gate time may be adjusted for .1s, 1s, or 10 sec.

Figure 9D-3-6. Making Period Average Measurements



1. Connect ac power to 5300A ac receptacle.

2. Turn ac power "on" with 5300A SAMPLE RATE control. Adjust sample rate for desired display time.

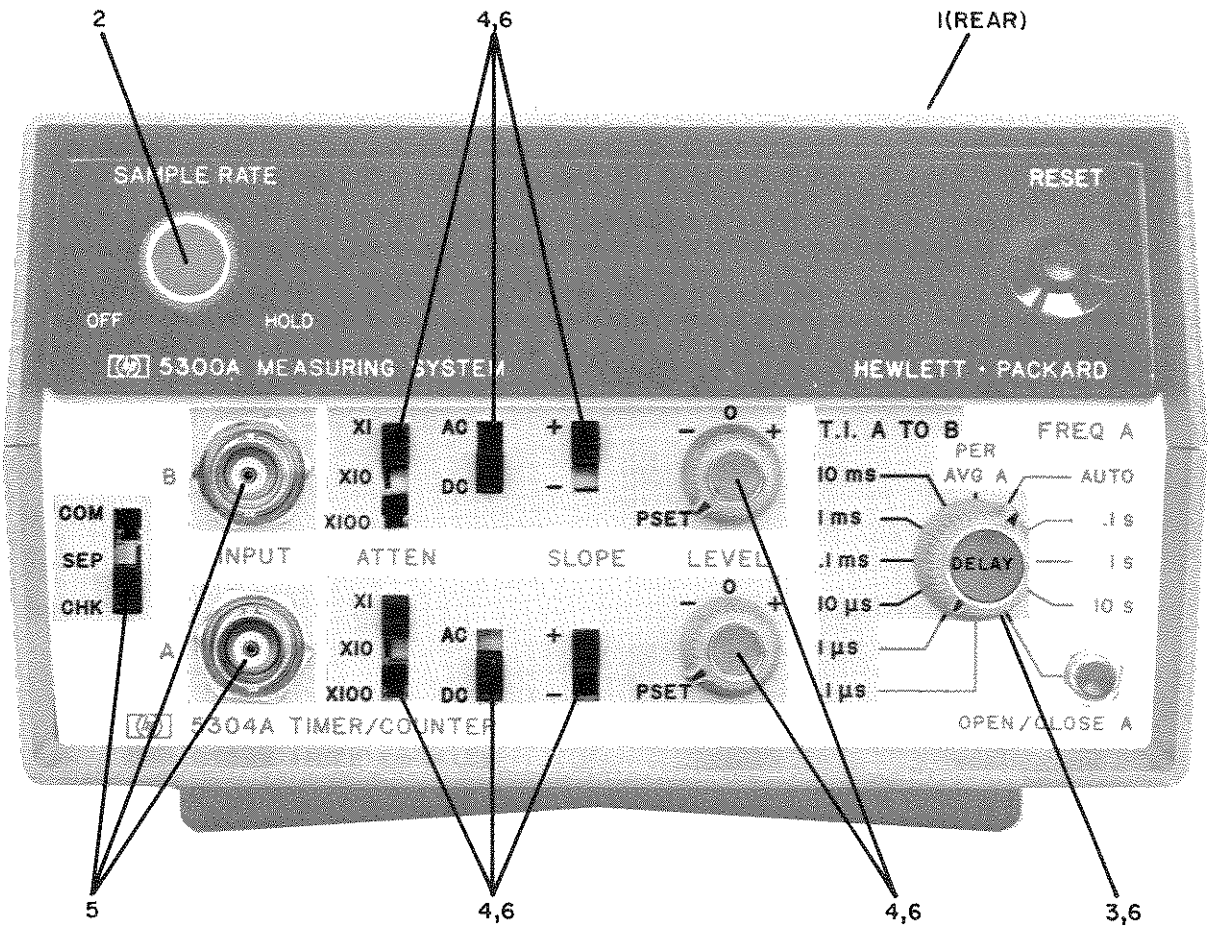
3. Set COM-SEP-CHK to SEP.

4. Connect input signal to INPUT A jack.

5. Set ATTEN to X100, AC-DC to coupling desired and SLOPE to polarity desired. Set LEVEL to PSET.

6. Set "Function" to PER AVG A; adjust ATTEN switch until a stable display is obtained. The number of periods averaged is automatically selected.

Figure 9D-3-7. Making Time Interval Measurements



1. Connect ac power to 5300A ac receptacle.

2. Turn ac power "on" with 5300A SAMPLE RATE control. Adjust sample rate for desired display time.

3. Set "Function" switch to T.I. A to B, with desired resolution. Ensure DELAY control is full ccw.

4. Set ATTEN switches for both channels to X100; AC-DC switches and SLOPE controls switches to settings desired; set LEVEL controls to PSET.

5. If Start and Stop signals are from separate sources, connect the Start signal to INPUT A connector and the Stop signal to INPUT B connector, then set the COM-SEP-CHK switch to SEP. If the Start and Stop signals are from a common source, connect the signal input to INPUT A and set the COM-SEP-CHK switch to COM.

6. Adjust ATTEN switches until a stable display is obtained.

7. Time Interval Holdoff (DELAY). The DELAY control inserts a delay of about 100 µsec to 100 msec between the triggering of the START Channel "A" and the enabling of the STOP Channel "B" (see Figure B). This delay may be used to measure relay or other mechanical switch timing sequences without error due to contact bounce. It may also be used for measurements on pulse trains; for example from the start pulse to a later pulse, in the presence of intervening pulses. To use the DELAY, proceed as follows:

   a. If the desired delay is known, it may be set and measured by selecting T.I. A to B and CHK and setting DELAY control to the desired delay time. The measurement may then be made by switching COM-SEP-CHK in step 5.

Figure 9D-3-7. Making Time Interval Measurements (Continued)

b. If the input signals are pulse trains, it is possible to select a pulse out of the train by increasing the DELAY from full ccw; the measured time interval will increase in steps as the delay falls after successive pulses in the train.

c. For maximum flexibility and ease of interpretation, an oscilloscope may be used to set up the measurement (as shown in Figure A). The DELAY OUTPUT is used to trigger the time base and intensity modulate the display (see Figure A). For a repetitive waveform, the Channel A input may fall during the display cycle, and therefore might not initiate a measurement. The GATE output may be substituted for the DELAY OUTPUT; this allows intensifying the actual measurement rather than the delay. If the inputs are common, the GATE OUTPUT or DELAY OUTPUT can be displayed on the second channel (or a third channel of a four-channel scope), and the other of these two used to intensity modulate.

d. Set oscilloscope controls as follows:

HP 1801A: Set A and B Channel controls for a display of both input signal. Set DISPLAY to A+B.

HP 1821A: Set TRIGGER to EXT. SLOPE to -.
Coupling to ACF.
SWEEP MODE to NORM.
Time/CM for one cycle of measured Time Interval.

e. Set DELAY slightly out of full ccw and select the time interval delay. The SWEEP TIME may have to be readjusted.

f. Adjust INTENSITY to view only the time interval measured.

g. Oscilloscope time display and 5300A time readout should be the same.

Figure B: Example of Delay Control

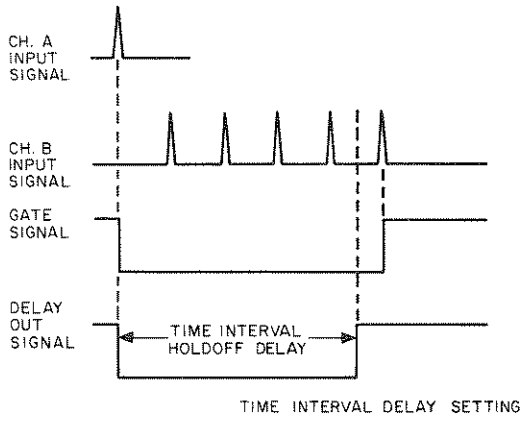


Figure A: Delay Control Setup

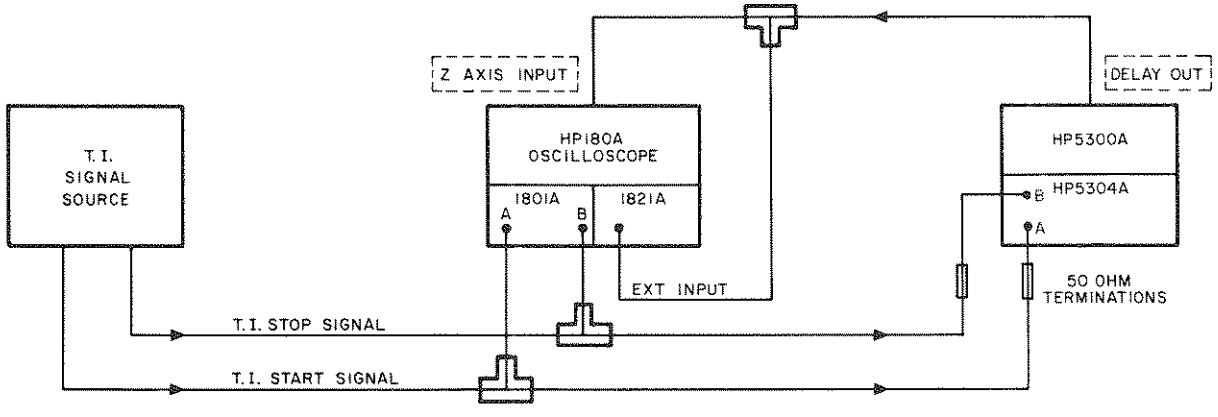
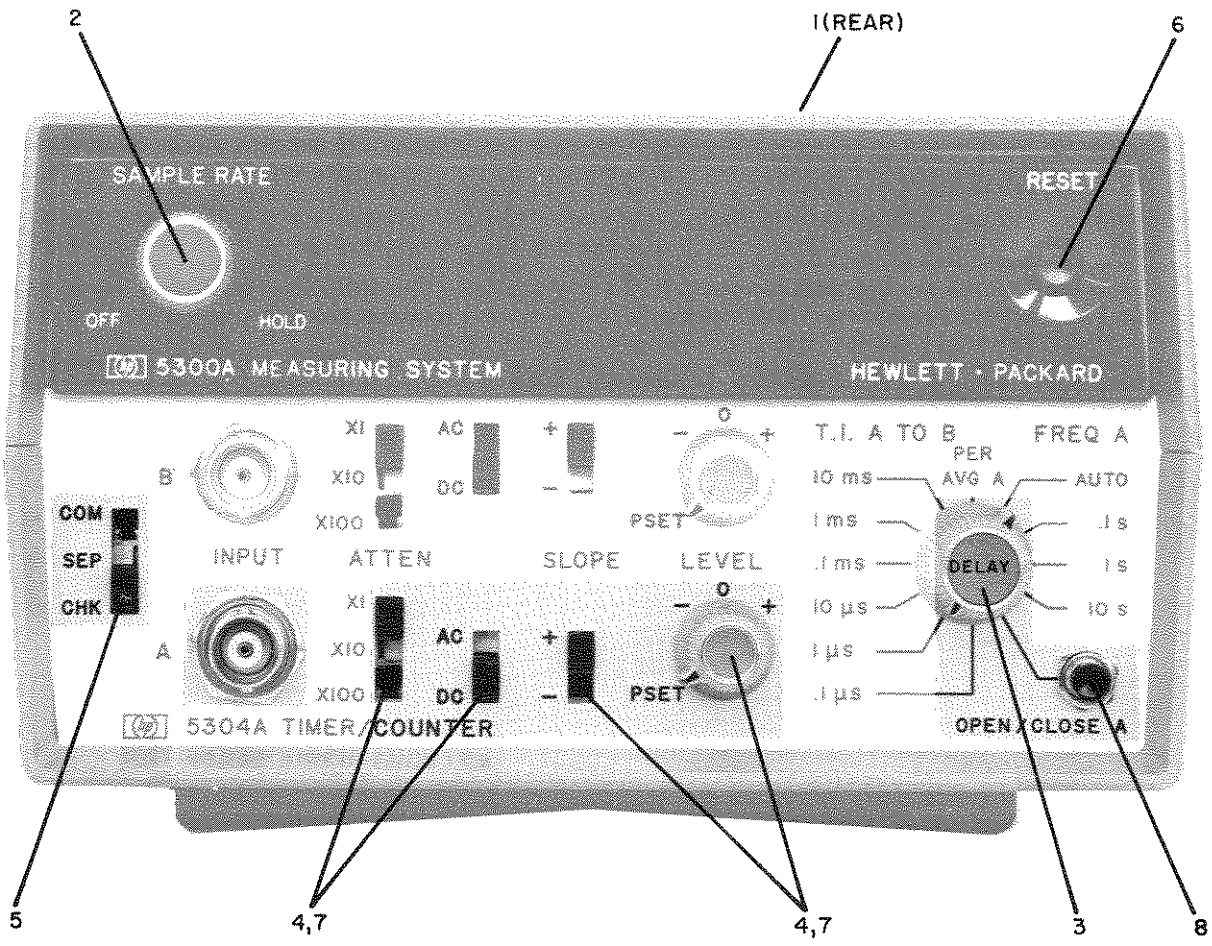


Figure 9D-3-8. Totalizing



1. Connect ac power to 5300A ac receptacle.

2. Turn ac power "on" with 5300A SAMPLE RATE control. Adjust sample rate for desired display time.

3. Set "Function" switch to OPEN/CLOSE A.

4. Set Channel A ATTEN to X100; AC-DC and SLOPE to desired positions. Set LEVEL to PSET.

5. Connect signal to be totalized to INPUT A; set COM-SEP-CHK to SEP.

6. Press RESET; press OPEN/CLOSE A switch; C lamp should come on.

7. Reduce ATTEN A until counting occurs. Display will accumulate at a rate dependent on input signal frequency.

8. When the display has accumulated the desired number of counts, press OPEN/CLOSE A switch to stop totalizing.

9. If the operator wants to totalize starting from the number accumulated in the display, press the OPEN/CLOSE A switch. If a new totalizing measurement is to be made, press RESET before pressing OPEN/CLOSE A switch.

SECTION IX D

5304A TIMER/COUNTER

SUBSECTION IV
THEORY OF OPERATION

9D-4-1. INTRODUCTION

9D-4-2. This subsection describes the theory of operation for the 5304A Timer/Counter. Basic operation of gates, certain amplifiers and integrated circuits is found in Section IV of the 5300A portion of the manual.

9D-4-3. To simplify measurement making refer to operating information starting with Paragraph 9D-3-1 for optimum adjustment of various controls.

9D-4-4. INPUT AMPLIFIERS AND MODES OF OPERATION

9D-4-5. CHANNEL A. The Channel A input signal is applied to front-panel INPUT A jack and attenuated by A2 attenuator assembly (X1, X10, X100) and sent to A1 Channel A input amplifier. The A2 Attenuator Board Assembly also contains the AC-DC switches, SLOPE switches, and the LEVEL controls for both channels. The input signal is sent through A2 to the input of matched FET source-follower pair, Q2 and Q4. Diodes CR2, CR4 are limiters for Q2 inputs.

9D-4-6. One side of the FET source-follower pair (Q2) receives the input signal from A2J2 and the other side (Q4) is connected to LEVEL A trigger-level control A2R9. Q2 and Q4 are connected to differential amplifier Q6 and Q8 respectively and provides level shifting and gain of approximately .3 for Channel A signals. Resistor R20 is a dc balance for differential amplifier Q6 and Q8.

9D-4-7. The output from Q6, Q8 drives another differential amplifier, U24B. The U24B output is shaped by Schmitt-Trigger U24A and level-shifted (ECL to TTL) through U21B, Q12 combination. The U21B expander output is used to obtain sufficient signal swing to drive Q12.

9D-4-8. CHANNEL B. The Channel B input signal is applied to front-panel INPUT B jack and attenuated by A2 Attenuator Assembly (X1, X10, X100) and sent to A1 Channel B input amplifier. The A2 Attenuator assembly also contains the Channel B coupling switches, slope switches and the Channel B level control. The Channel B signal is routed through A2 to the input of matched FET source-follower pair Q1 and Q3. Diodes CR1, CR3 are limiters for Q1 inputs.

9D-4-9. One side of the Channel B FET source-follower pair (Q1) receives the input signal from A2J1 and the other side (Q3) is connected to LEVEL B trigger level control A2R10. Q5 and Q7 are connected to differential amplifiers Q5 and Q7 respectively and provide level-shifting and gain of approximately .3 for Channel B signals. Resistor R19 is a dc balance for differential amplifier Q5 and Q7.

9D-4-10. The output from Q5, Q7 drives another differential amplifier U23B. The U23B output is shaped by Schmitt-Trigger U23A and level-shifted (ECL to TTL) through U21A, Q11 combination. The U21A expander output is used to obtain sufficient signal swing to drive Q11.

9D-4-11. VOLTAGE REGULATION. Transistors Q9, Q10 provide regulated, low-ripple dc power to the amplifiers and time interval hold-off circuits.

9D-4-12. SLOPE SELECTION. Slope selection for Channel A is accomplished by using U19C, U20C, and U20D in conjunction with A2S7. Slope selection for Channel B is accomplished by using U19D, U20D, and U20A in conjunction with A2S6.

9D-4-13. CHECK MODE. In the CHECK mode, the operation of the 5300A 10 MHz crystal oscillator and counting logic and the 5304A gating logic is verified. When A2S1 is in CHK mode, ground is applied to U18A(2), U18D(12), and U13C(5). The 10 MHz clock from the 5300A A1J1(16) is routed through the 5304A A1P1(16) and sent to U12D(12). The Channel A switch (U18B) and Channel B switch (U18C), gate the 10 MHz clock signal through. The Channel A switch output is also gated through U12B and U16B and is available as the F1 signal at A1P1(5).

9D-4-14. FREQ A MODE. In the frequency measuring mode, with the "Function" switch S2 in any of its four frequency measuring positions (FREQ AUTO, .1S, 1S, 10S) the Channel A input signal is gated through "Channel A Slope Selection" switch comprised of U19C, U20C, and U20B. The input signal is then routed through another "Channel A" switch made up of U18A and U18B. From U18B(6) the Channel A input signal is gated through U12B and U16B as the F1 signal to the 5300A mainframe which controls the opening and closing of the main gate. The 10 MHz clock signal from

the 5300A mainframe at A1P1(16) is routed through U12C as the F2 signal to control the time base, which clocks the opening and closing of the main gate.

9D-4-15. The positive-going edge of a negative pulse from U17E is the $\overline{\text{MAX TIME}}$ signal. The $\overline{\text{MAX TIME}}$ signal at A1P1(17) triggers a display cycle in the 5300A mainframe. This negative-going pulse can be generated from one of two sources. One of the sources is the positive-going edge of the $\overline{\text{MGFF}}$ line at A1P1(12) which indicates the closing of the 5300A main gate. This signal is inverted through U17D and differentiated by C14 and R69. CR18 is a clamping diode to shorten the differentiation recovery time. The negative pulse of the differentiated waveform, gates U16A "on" and the narrow positive-going pulse is inverted through U17E as the $\overline{\text{MAX TIME}}$ signal.

9D-4-16. The TIME BASE OUT signal at A1P1(18) comes from the 5300A mainframe and is buffered by Q18 then gated through U14C, U16A, and inverted through U17E as the $\overline{\text{MAX TIME}}$ signal.

9D-4-17. The positive-going edge of the negative pulse at A1P1(17), indicates the display cycle has been triggered.

9D-4-18. PERIOD AVG A MODE. In period average mode the "function" switch S2 enables U1A, U6D, U12C, and U14A. The Channel A signal is routed through "Channel A Slope Selection" and "Channel A Switch" at U18B(6). The signal is then gated through U16C and is available at A1P1(21) as the 1 MHz TIME BASE. The CLOCK signal at A1P1(16) is gated through U12A, U16B as the F1 signal to be counted.

9D4-19. Flip-flop U4A prevents very narrow pulses from triggering the time base but not the main gate. The first Channel A pulse after the INHIBIT signal goes high at the end of the display cycle "clocks" U4A(5) to a high state and enables U16C. The next positive-going edge of the Channel A signal is gated through U16C as the 1 MHz TIME BASE INPUT signal. The main gate is then closed by one of two events. The first event is: The 9 signal line from 5300A, U3 COUNTER, goes low, and enables the main gate in the 5300A, U5 CONTROL, to close on the next LOG pulse. When the 9 line goes low it indicates that the display is 9% full. The main gate closes at the end of the next decade-multiple of the input signal to prevent overflow. The second event is: The TIME BASE OUT signal (A1P1(18)) from the 5300A, U4 TIME BASE goes low indicating the 10^3 periods have been counted. The main gate closes because no more counts can be stored in the 5304A exponent counter U8A and U8B. The exponent counter counts the number of decade-transitions of the input signal that have been counted (1, 10, 100, 1000 input transitions or exponent counts of 1, 2, 3, 4).

9D-4-20. The $\overline{\text{LOG OUTPUT}}$ signal (generated by 5300A, U4 TIME BASE) is active in Frequency and Period Average Modes and provides pulses to open and close the main gate. Following a display cycle and reset, the first $\overline{\text{LOG}}$ pulse opens the main gate and a following $\overline{\text{LOG}}$ pulse will close the gate only after a $\overline{9}$ or $\overline{\text{MAX TIME}}$ low signal enables the closing of the main gate flip-flop.

9D-4-21. OPEN/CLOSE A MODE. In open/close mode, with the "function" switch S2 in OPEN/CLOSE position the main gate is opened and closed by successive actuations of pushbutton switch S1. The Channel A input signal is gated through "Slope Selection" switch U19C, U20B, and U20C to "Channel A Switch" U18A and U18B.

9D-4-22. The Channel A input signal is gated through U12B, U16B to be counted. U4B "clocks" on successive actuations of the S1 OPEN/CLOSE switch. When U8B(9) output is low the 5300A main gate is opened (through U19B). When U4B(8) output is low the 5300A main gate is closed (through U14D and U22A). When the "Function" switch S2 is in a position other than OPEN/CLOSE, the U4B Preset and Clear lines (U4B pins 10 and 13 respectively) are set through U10A and B, so that U4B, Q and Q output (U4 pins 9 and 8) are high.

9D-4-23. TIME INTERVAL A-B MODE. In the time interval mode, the "function" switch S2 may be set to any one of six time-interval positions (.1 μsec to 10 msec). The 5300A main gate is opened by a Channel A transition and closed by a Channel B transition. Switch A2S1 enables the input signals to be taken from separate sources or from a common source.

9D-4-24. The Channel A signal, after passing through A2 Attenuator Assembly, is processed through Channel A amplifier, Q2 Q4 and differntial amplifiers Q6, Q8, and U24B. The U24B output is shaped through U24A Schmitt-Trigger and sent through an ECL-to-TTL level-shifter (U21B, Q21) to the Channel A Slope Selection circuits (U19C, U20C, U20B).

9D-4-25. The output from U20B(4) is gated through Channel A switch, comprised of U18A and B. The Channel A signal "clocks" U15B which is gated through U9C, U19B, and opens the 5300A main gate. During the gate-open time, the TIME BASE OUT

signal from the 5300A A1J1(18) is gated through Q18, U17F, U9B, and U16B to be counted (except in the .1 μsec position, where the 10 MHz clock is gated through U12A and U16B). The TIME BASE OUTPUT signal is a 10 MHz clock signal divided down by the time base to allow counting in increments of 1 μsec, 10 μsec etc.

9D-4-26. The main gate closes when Channel B "clocks" U15A and a display cycle is initiated by the positive-going edge of the MGFF signal at A1P1(12). This signal is inverted through U17D and differentiated by C14 and R69. The negative pulse of the differentiated waveform gates U16A "on" and the narrow positive-going pulse is inverted through U17E as the $\overline{\text{MAX TIME}}$ signal.

9D-4-27. At the end of the display cycle, the RESET signal at A1P1(15) is inverted through U13E and sets U15B(9) low. U15A(5) is set high by the PRESET signal at U15A(4). The $\overline{\text{INHIBIT}}$ signal goes "high" and sets U15B(12) so that U15B changes states on the positive-going transition from U18B(6). This produces two results:

1. U9C(8) goes low which set the $\overline{\text{OPEN}}$ signal at A1P1(10) low through U19B and opens the 5300A main gate.

2. Q16 turns off and allows C12 to charge through R43 and R61.

9D-4-28. Transistor Q15 is an emitter-follower input to Schmitt-Trigger Q13, Q14. The output from Q13 is level-shifted by CR15 and inverted by Q17. Q15, 14, 13, and 17 form a one-shot multivibrator with a very wide timing range. U15A cannot change states until Q17 output goes low; then U15A(3) is clocked to its opposite state by the positive transition of U18C (Channel B switch output). The U15A(5) output is gated and inverted through U14D and U22A. This causes the $\overline{\text{CLOSE}}$ signal line to go low which in turn closes the 5300A main gate.

9D-4-29. The 5300A main gate cannot be re-opened until U15B is cleared by the RESET signal at A1P1(15) and until the $\overline{\text{INHIBIT}}$ signal at A1P1(8) sets U15B(12) high. U15B(8) goes high at RESET and turns on Q16 which discharges C12. When R43(S2) is open (full ccw), C12 is not charged up and the one-shot time-interval is very short (about 200 nsec). The time-interval is the interval from the time U15B(8) goes low and Q17 collector goes low.

9D-4-30. A buffered DELAY OUT signal is provided at J3 and may be used for intensifying the oscilloscope Z axis which permits observing the start and stop period in a time interval measurement. A buffered GATE OUT signal is also provided at J4 which permits observing the gate signal duration in a time interval measurement.

9D-4-31. EXPONENT COUNTER; EXPONENT STORAGE. Outputs from the 5300A, U5 $\overline{\text{EXP}}$ line are applied to exponent counter U8A, U8B "Clock input". The RESET signal at A1P1(15) clears U8A and presets U8B for another measurement. Exponent signals "clocked" into U8 indicate length of measurements (10 ms, 100 ms, or 1 sec in FREQ AUTO mode; 1, 10, 100, 1000 periods in PERIOD AVG mode). During the measurement cycle, information is transferred into U7A, B exponent storage by the $\overline{\text{TRANSFER}}$ signal. Therefore, the displayed measurement, the decimal point and the units, change simultaneously.

9D-4-32. Exponent storage U7A, B is disabled (both flip-flops are cleared), except in AUTO measurements, by U6D. Manual reset also clears U7A, U7B, the decimal point and measurement units.

9D-4-33. The remainder of the gates with the exception of U5B provide time base, decimal point, annunciator, and function decoding. The U3A output is high in any of the four frequency-measuring positions. U5B locks out the $\overline{\text{LOG OUTPUT}}$ signal in OPEN/CLOSE A and TIME INTERVAL A-B, when the open and closing of the main gate is controlled by $\overline{\text{OPEN}}$ and $\overline{\text{CLOSE}}$.

9D-4-34. Q19 normally turns off the 9 line except during frequency Auto or Period Average; this allows overflow to occur, if desired, in manual frequency position.

SECTION IX D
5304A TIMER/COUNTER

SUBSECTION V
MAINTENANCE

9D-5-1. INTRODUCTION

9D-5-2. This section contains maintenance and service information for Model 5300A/5304A Timer/Counter. Included are performance check procedures and tests to localize, isolate, and locate defective components.

9D-5-3. RECOMMENDED TEST EQUIPMENT

9D-5-4. Test equipment recommended for performance checks, maintaining, troubleshooting and servicing the 5300A/5304A Timer/Counter is listed in Table 5-1 of 5300A portion of the manual. Test equipment with equivalent characteristics may be substituted for equipment listed.

9D-5-5. INSTRUMENT ACCESS

9D-5-6. For access to plug-on assembly, separate the 5300A from the 5304A as follows:

a. Turn ac power OFF and disconnect power cord.

b. Pull the two-side casting latches fully rearward (it is necessary to press the latch handles gently away from the center of the instrument to unlock them).

c. When latches are fully extended rearward, the 5300A and 5304A castings should be separated by about ⅛-inch.

d. Lift the 5300A gently away from the 5304A.

e. Separate 5304A A1 BOARD ASSEMBLY from 5304A casting as follows (refer to Figure 9D-5-1):

1. Press rear, plastic-nylon retaining clips on each side of 5304A casting and lift the rear of the A1 Board Assembly to release it from the casting.
2. Press front plastic-nylon retaining clips on each side of 5304A casting and lift the front of the A1 Board Assembly to release it from the casting.
3. Lift A1 Board Assembly from the casting.

f. Mate the 5304A, A1 Board Assembly to 5300A and reapply ac power.

g. To reinstall the A1 Board Assembly into the casting reverse procedure of steps d through f.

9D-5-7. PERIODIC MAINTENANCE

9D-5-8. To determine if the 5300A/5304A is operating properly within specifications, perform the In-Cabinet Performance Checks listed in Table 9D-5-1. These checks may also be used for the 5300A performance checks when the 5300A/5304A combination is used.

9D-5-9. MAINTENANCE AND REPAIR

9D-5-10. BOARD REMOVAL. When removing the printed circuit board for replacement, repair, or servicing, always remove ac power and separate the board from the casting using Paragraph 9D-5-6 steps a to e.

9D-5-11. COMPONENT REPLACEMENT. When replacing a circuit board component use a low heat soldering iron. Heat must be used sparingly as damage to the circuit foil may result. Mounting holes may be cleaned out with a toothpick while heat is applied. Connection should be cleaned with a cleaning solution after component removal and replacement.

9D-5-12. INTEGRATED CIRCUIT REPLACEMENT. Two methods are recommended for removing integrated circuits:

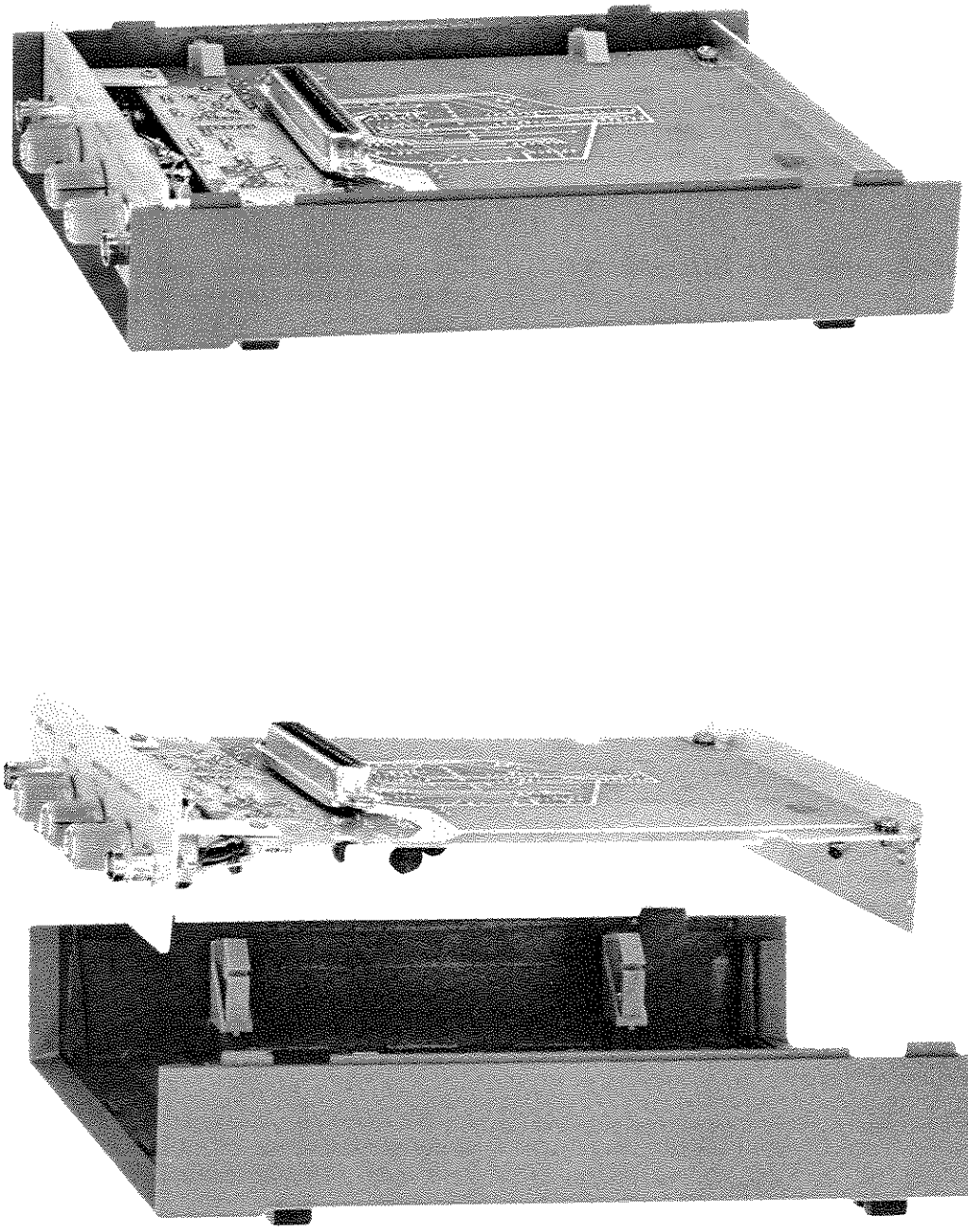
a. Solder Gobbler. Solder is removed from board by a soldering iron with a hollow tip connected to a vacuum source. The IC is removed intact so it may be reinstalled if diagnosis is wrong.

b. Clip-Out. This method is used when an IC is proven defective. Clip leads close to case, apply heat and remove leads with long nose pliers. Clean board holes with a toothpick and cleaning solution.

9D-5-13. INSTRUMENT TROUBLESHOOTING

9D-5-14. Trouble isolation can best be accomplished by first obtaining all possible information from the controls, connectors, and indicators on the 5300A and 5304A, then logically using this information to locate the defective component. If the

Figure 9D-5-1. Separation Procedure



performance checks indicate a malfunction or if instrument operation is suspect, perform the Self-Check procedures in Table 9D-5-1. For further tests, separate the 5304A from the casting and reconnect to 5300A using Paragraph 9D-5-6 steps a to e as a guide. Operating procedures in Subsection 9D-3 can be used to help understand operation. To test the 5304A, obtain the test equipment listed in Table 5-1 of the 5300A portion of the manual.

9D-5-15. Figure 9D-5-2 to Figure 9D-5-6 are troubleshooting flow diagrams for each of the five modes of operation. Signal flow is outlined for each mode and waveform test points and voltage test points are indicated. The waveforms or voltage level for each mode is included with the figures. To obtain the waveforms and/or levels for each mode, follow the directions for instrument connections which are listed with the troubleshooting flow diagrams of each respective mode.

9D-5-16. DC BALANCE ADJUSTMENT

9D-5-17. If Channel A or Channel B fail to operate with their respective LEVEL controls in PSET position when measuring sine wave signals, or when periodic maintenance/calibration is performed, the dc balance may be adjusted as follows:

a. Connect an HP 651B Oscillator, set to 10 MHz, 50 mV rms/50Ω, through a 50 OHM BNC Feed-thru Termination, to Channel A input.

b. Set the 5304A controls as follows:

ATTEN to X1 (both channels).
AC-DC to AC (both channels).
+, - to + (both channels).
LEVEL to PSET (both channels).
SEP-CHK to SEP
"Function" to FREQ A, AUTO

c. Connect an HP 180A oscilloscope through a 10 MΩ probe to U18(6).

d. Adjust the oscilloscope controls to monitor a useable signal.

e. Adjust A1R20 for a symmetrical waveform with minimum or no change in duty-cycle when SLOPE switch is changed from + to - and minimum or no change when AC-DC switch is set to AC or DC.

f. Connect the oscilloscope probe to U18(8) and the 651B input signal to Channel B.

g. Adjust A1R19 for a similar display observed in step e.

FREQ A, AUTO MODE.

5304A controls:

Channel A, SEP, X1, AC, +, PSET, AUTO

INPUT:

HP 651B set to 10 MHz, 100 mV rms/50Ω.

Oscilloscope:

HP 180A, 1801A Vert. Amp. 1821A T.B. through a 10:1 probe.

Settings:

AC coupled (except as noted).
NORM sweep mode.
+ SLOPE (except as noted).
ACF (except as noted).
Channel A.

5300A SAMPLE RATE ccw out of OFF (except as noted). 5300 Display should be approximately the same as the HP 651B setting.

Test points using HP 10525A Logic Probe

H = High (lamp on)

L = Low (lamp off)

TP1 H (dim). Flash rate decreases as 5300 SAMPLE RATE control is truned cw.

TP2 H (dim). Flash rate decreases as 5300 SAMPLE RATE control is turned cw. Level goes Low when 5300A RESET is pressed.

TP3 H (dim). Flash rate decreases as 5300A SAMPLE RATE control is turned cw. Level goes Low when 5300A RESET is pressed.

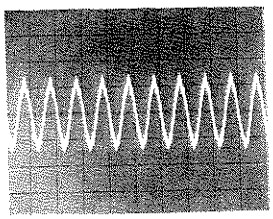
TP4 H (dim). Flash rate decreases as 5300A SAMPLE RATE control is turned cw. Level goes High when 5300A RESET is pressed.

TP5 H (dim). Flash rate decreases as 5300A SAMPLE RATE control is turned cw. Level goes High when 5300A RESET is pressed.

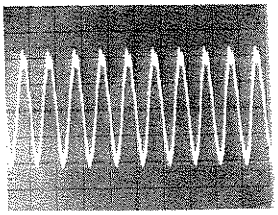
TP6 L. Goes High when 5300 RESET is pressed.

TP7 L. Goes High when 5300A RESET is pressed.

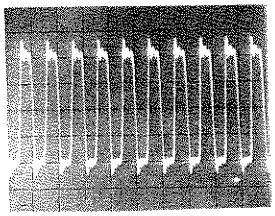
TP8 L.



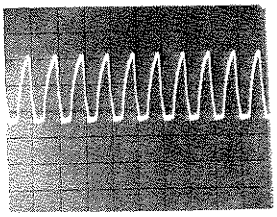
1 .01 V/cm
.1μsec/cm



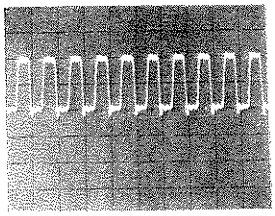
2 .01 V/cm
.1μsec/cm



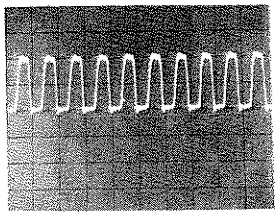
3 .01 V/cm
.1μsec/cm



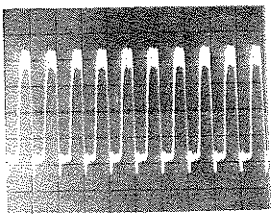
4 .2 V/cm
.1μsec/cm
dc coupled



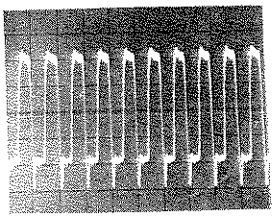
5 .2 V/cm
.1μsec/cm
dc coupled



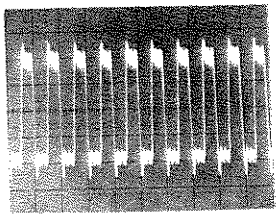
6 .2 V/cm
.1μsec/cm
dc coupled



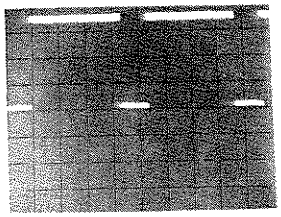
7 .1 V/cm
.1μsec/cm



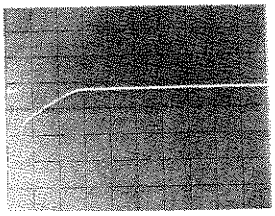
8 .1 V/cm
.1μsec/cm



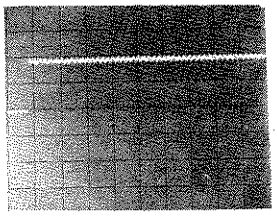
9 .1 V/cm
.1μsec/cm



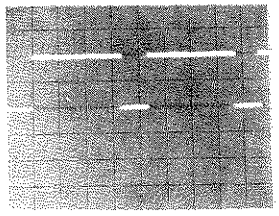
10 .1 V/cm
10 msec/cm
dc coupled
- slope



11 .2 V/cm
.2μsec/cm
dc coupled
- slope



12 .2 V/cm
.5μsec/cm
dc coupled
- slope



13 .2 V/cm
10 msec/cm
dc coupled
- slope

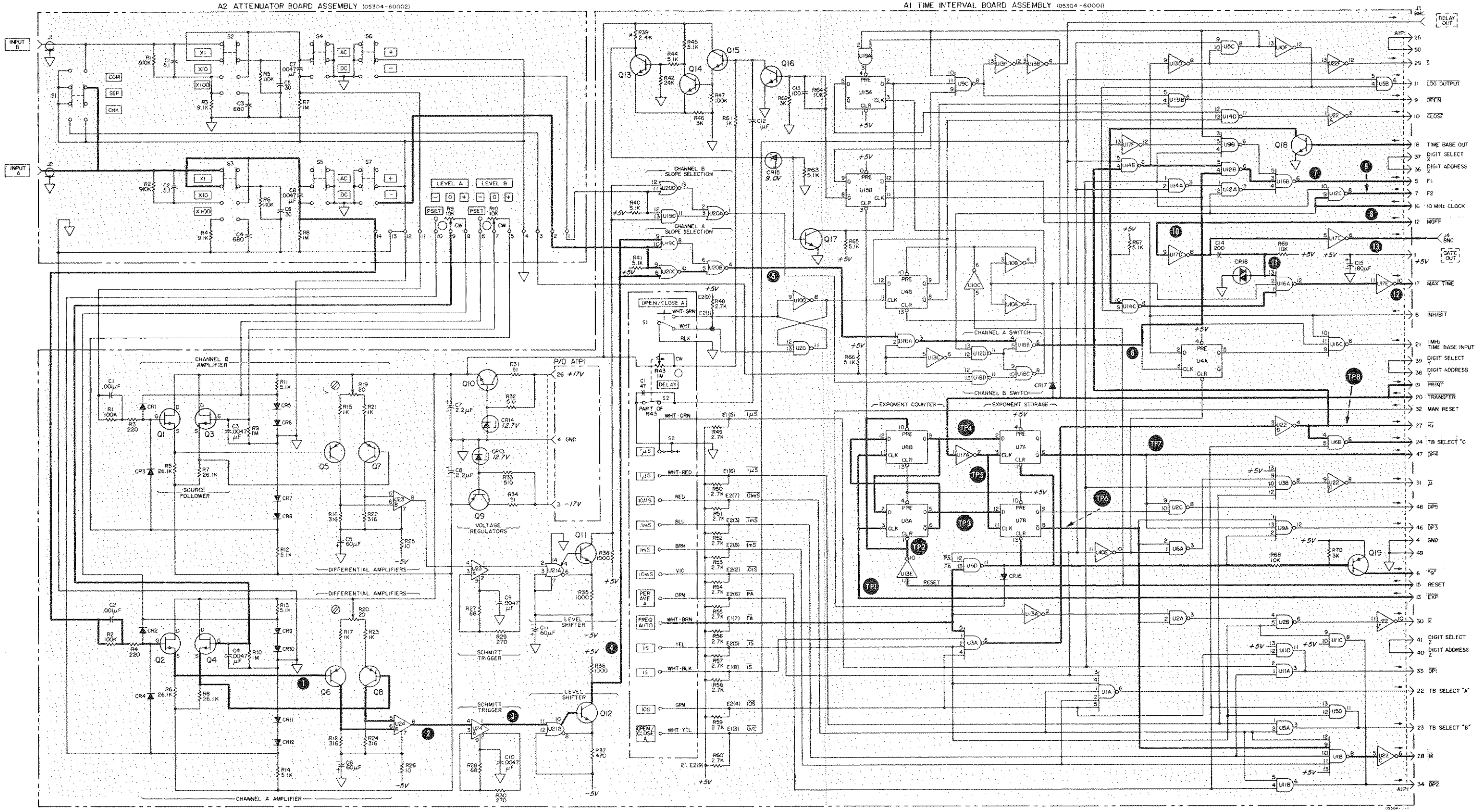


Figure 9D-5-2. Frequency A Troubleshooting Diagram

FI
FREQUENCY A TROUBLESHOOTING
(See F

PERIOD AVERAGE A MODE

5304A Controls:

Channel A, SEP, X1, AC, +, PSET, PER AVG A.

INPUT:

651B set to 1 kHz, 100 mV rms/50Ω.

Oscilloscope:

HP 180A, 1801A Vert Amp, 1821A T.B. through a 10:1 probe.

Settings:

AC coupled (except as noted).
NORM sweep mode.
+ slope (except as noted).
Channel A.

5300A

SAMPLE RATE ccw out of OFF (except as noted). 5300 Display should be approximately 1.00000 MS, C.

HP 10525A Logic Probe

Test points using

H = High (lamp on)

L = Low (lamp off)

TP1 H (dim). Flash rate decreases when 5300 SAMPLE RATE is turned cw. Goes Low when RESET is pressed.

TP2 H (dim). Flash rate decreases when 5300 SAMPLE RATE is turned cw. Goes Low when RESET is pressed.

TP3 H (dim). Flash rate decreases when 5300 SAMPLE RATE is turned cw. Goes High (bright) when RESET is pressed.

TP4 H (dim). Flash rate decreases when 5300 SAMPLE RATE is turned cw. Goes High (bright) when RESET is pressed.

TP5 L. Goes High when RESET is pressed.

TP6 H

TP7 H

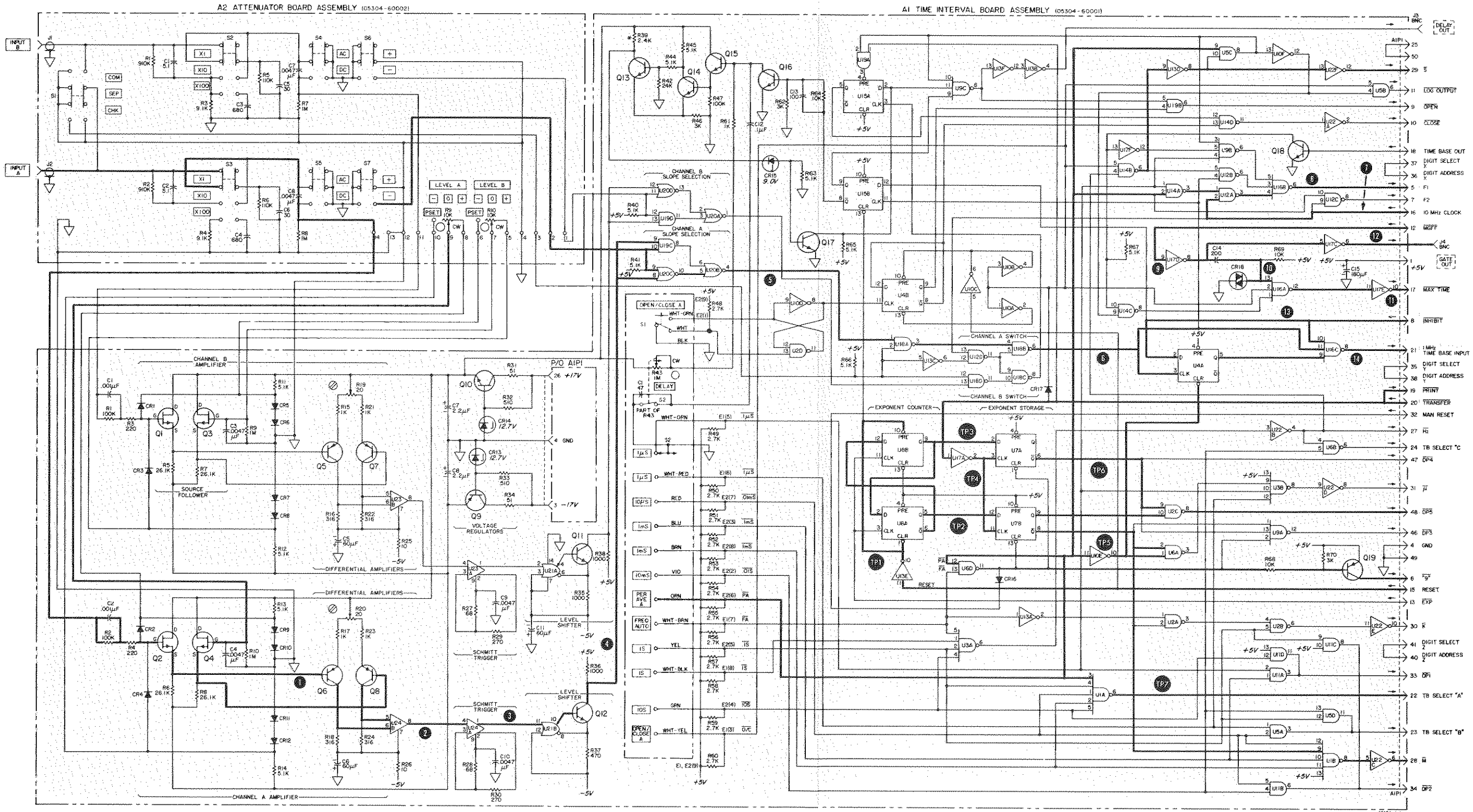


Figure 9D-5-3. Period Average A Troubleshooting Diagram

Fig

PERIOD AVERAGE A TROUBLESHOOTING

(See P

TIME INTERVAL A TO B Mode, .1 μsec position.

Equipment connections: Connect equipment as shown in Figure 9D-5-4A.

Control Settings: 5300/5304A.

ATTEN (both channels) to X1.
AC-DC (both channels) to DC.
SLOPE (both channels) to +.
LEVEL. Set Channel A LEVEL slightly positive (+) until the "C" lamp comes on. Set Channel B LEVEL cw until a stable 5300 display is obtained.
Function to .1 μsec.
COM/SEP/CHK to SEP.

Oscilloscope:

VOLTS/CM to 2 (both channels).
DISPLAY to A + B.
INPUT (both channels) to DC.
TIME/CM to 1 μsec.
SWEEP MODE to NORM.
TRIGGER to INT.
SLOPE to +.
Coupling to ACF or AC.

No. 1 HP 222A:

REP RATE to 1K-10K with adjustment centered.

PULSE DELAY has no effect.

PULSE WIDTH to .05-.5. Vernier adjusted for oscilloscope display of .1 μsec.

PULSE POLARITY to +.

PULSE AMPLITUDE for a +2 V pulse on oscilloscope.

No. 2 HP 222A:

REP RATE to MAN/EXT +.

PULSE WIDTH to .05-.5. Vernier adjusted for oscilloscope display of .1 μsec.

PULSE POLARITY to +.

PULSE AMPLITUDE for a +2 V pulse on oscilloscope.

PULSE DELAY for approximate display, on oscilloscope and 5300A, of 10 μsec (5300 display should be approximately 00010.0 μs C).

From the set-up outlined in Figure 9D-5-4A, disconnect the Channel A input to the HP 180A Oscilloscope. Connect a 10:1 divider probe and check for the waveforms listed.

Test points using an HP 10525A Logic Probe

H = High (lamp on)

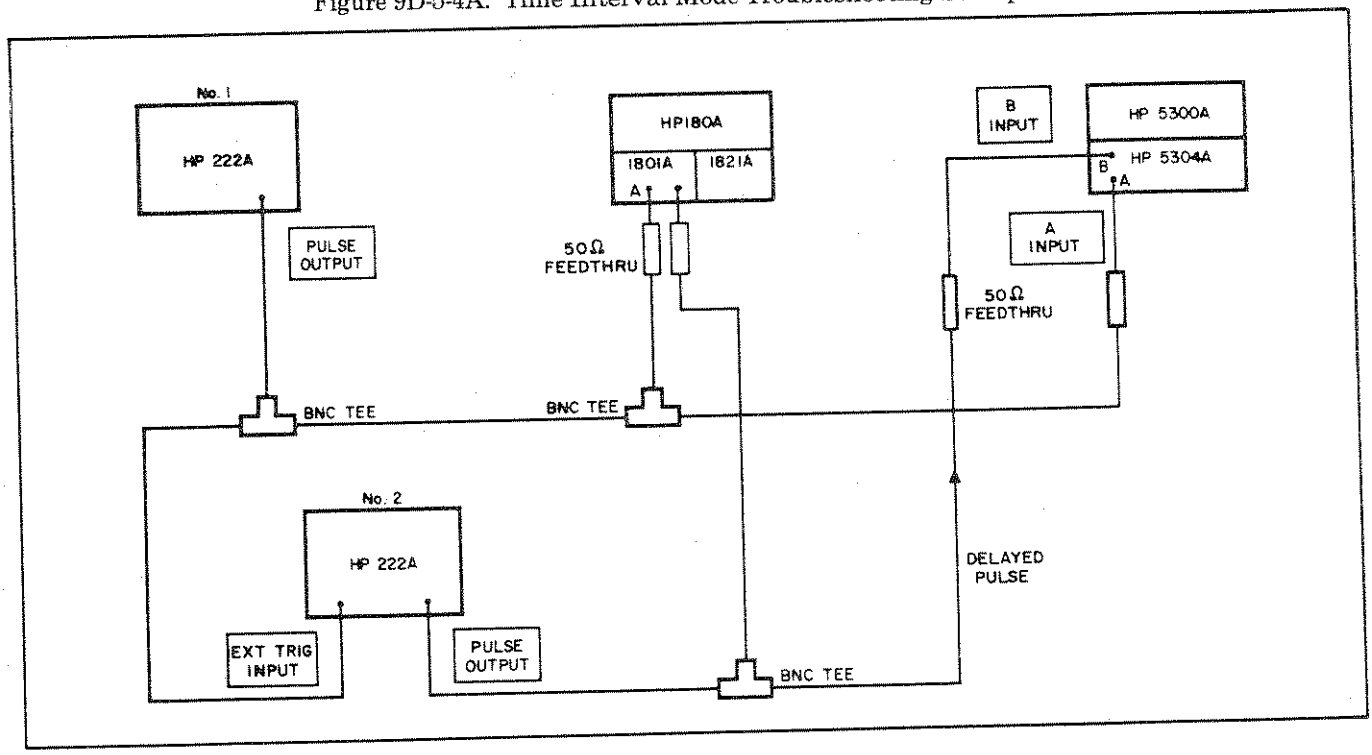
L = Low (lamp off)

TP1 H (dim). Flash rate decreases when DELAY control is turned cw or when SAMPLE RATE is turned cw.

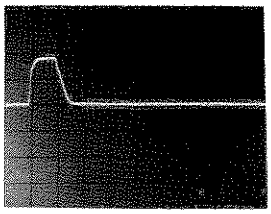
TP2 H (dim). Flash rate decreases when DELAY control is turned cw or when SAMPLE RATE is turned cw.

TP3 H (dim). Flash rate decreases when DELAY control is turned cw or when SAMPLE RATE turned cw.

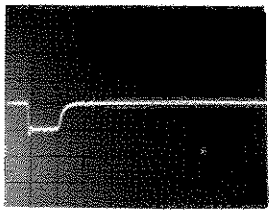
Figure 9D-5-4A. Time Interval Mode Troubleshooting Set-Up



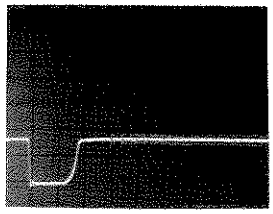
Part of Figure 9D-5-4. Time Interval Troubleshooting Diagram



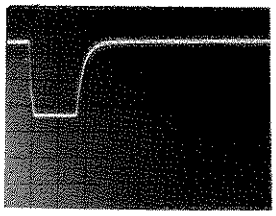
❶ .1 V/cm
.1 μsec/cm



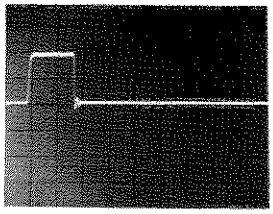
❷ .05 V/cm
.1 μsec/cm
- Slope



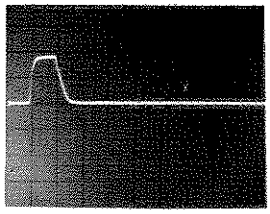
❸ .05 V/cm
.1 μsec/cm
dc coupled
- Slope



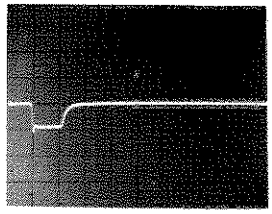
❹ .2 V/cm
.1 μsec/cm
dc coupled
- Slope



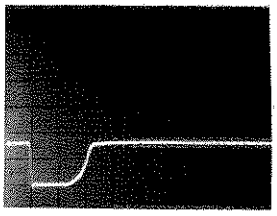
❺ .2 V/cm
.1 μsec/cm
dc coupled



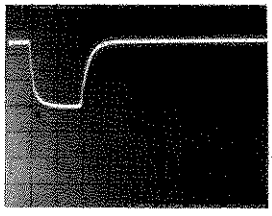
❻ .1 V/cm
.1 μsec/cm



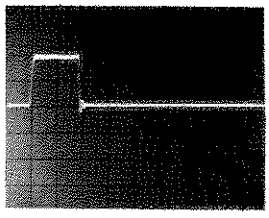
❼ .05 V/cm
.1 μsec/cm



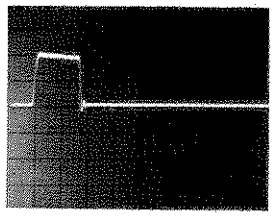
❽ .05 V/cm
.1 μsec/cm
dc coupled
- Slope



❾ .2 V/cm
.1 μsec/cm
dc coupled
- Slope

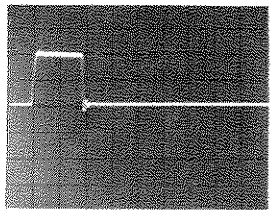


❿ .2 V/cm
.1 μsec/cm
dc coupled



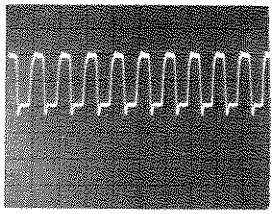
⓫ .2 V/cm
.1 μsec/cm
dc coupled

Part of Figure 9D-5-4. Time Interval Troubleshooting Diagram



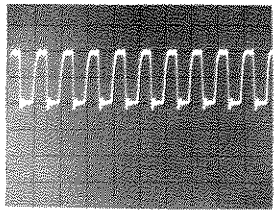
⑫

.2 V/cm
.1 μsec/cm
dc coupled



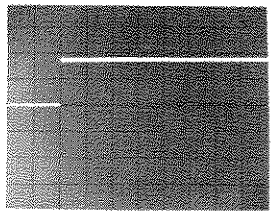
⑬

.2 V/cm
.1 μsec/cm
dc coupled



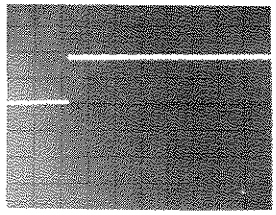
⑭

.2 V/cm
.1 μsec/cm
dc coupled



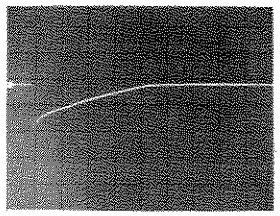
⑮ A

.2 V/cm
5 μsec/cm
dc coupled
- Slope
(DELAY IN DETENT)



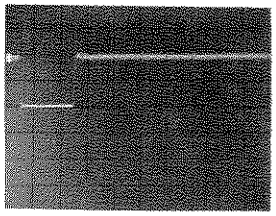
⑮ B

.2 V/cm
.1 msec/cm
dc coupled
- Slope
(DELAY just out of DETENT. 5300 Display and waveform should be the same)



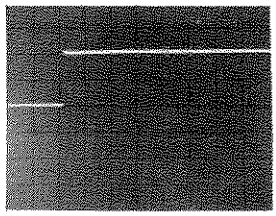
⑯

.2 V/cm
.1 μsec/cm
dc coupled
- Slope



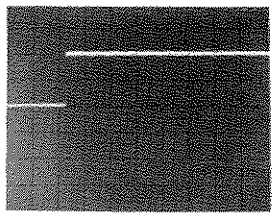
⑰

.2 V/cm
.2 μsec/cm
dc coupled
- Slope



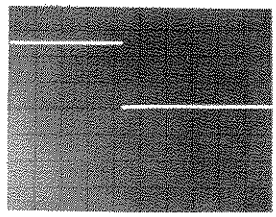
⑱ A

.2 V/cm
5 μsec/cm
dc coupled
- Slope
(DELAY IN DETENT)



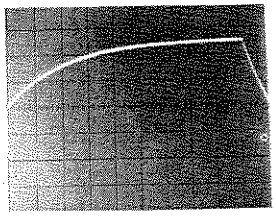
⑱ B

.2 V/cm
.1 msec/cm
dc cdoupled
- Slope
(DELAY just out of DETENT. 5300A Display and waveform should be the same)



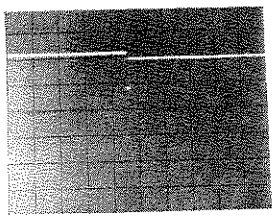
⑲ A

.5 V/cm
50 μsec/cm
dc coupled
(DELAY IN DETENT)



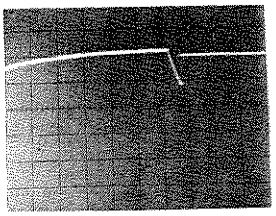
⑲ B

.5 V/cm
50 μsec/cm
dc coupled
(DELAY just out of DETENT. 5300ADisplay time should be approximateley one-half the oscilloscope waveform time)



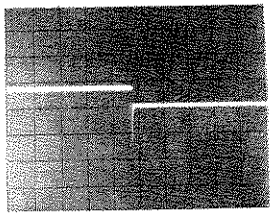
⑳ A

.5 V/cm
50 μsec/cm
dc coupled
(DELAY IN DETENT)



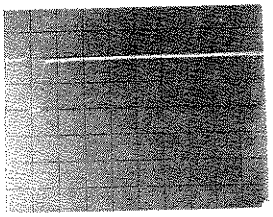
⑳ B

.5 V/cm
50 μsec/cm
dc coupled
(DELAY just out of DETENT. 5300A Display should be approximately 200 to 240 μsec)



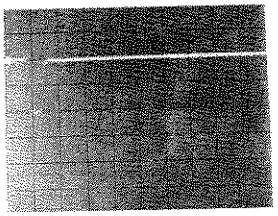
㉑

.1 V/cm
50 μsec/cm
dc coupled



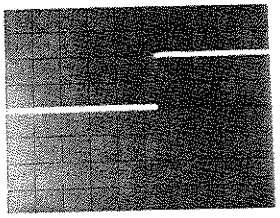
㉒

.2 V/cm
.1 μsec/cm
dc coupled
- Slope



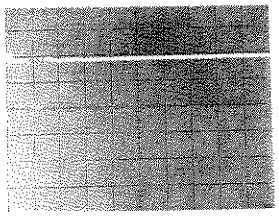
㉓ A

.2 V/cm
.1 μsec/cm
dc coupled
- Slope
(DELAY IN DETENT)



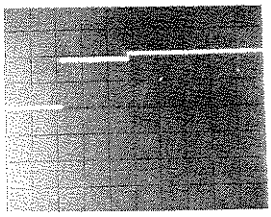
㉓

.2 V/cm
20 μsec/cm
dc coupled
- Slope
(DELAY just out of DETENT. 5300A Display should be approximately 200 to 240 μsec)



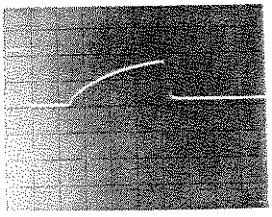
㉔ A

.2 V/cm
.1 μsec/cm
dc coupled
- Slope
(DELAY IN DETENT)



㉔ B

.2 V/cm
50 μsec/cm
dc coupled
- Slope
(DELAY just out of DETENT. 5300A Display should be approximately the total time of waveform pulse)



㉕

.2 V/cm
.1 μsec/cm
dc coupled

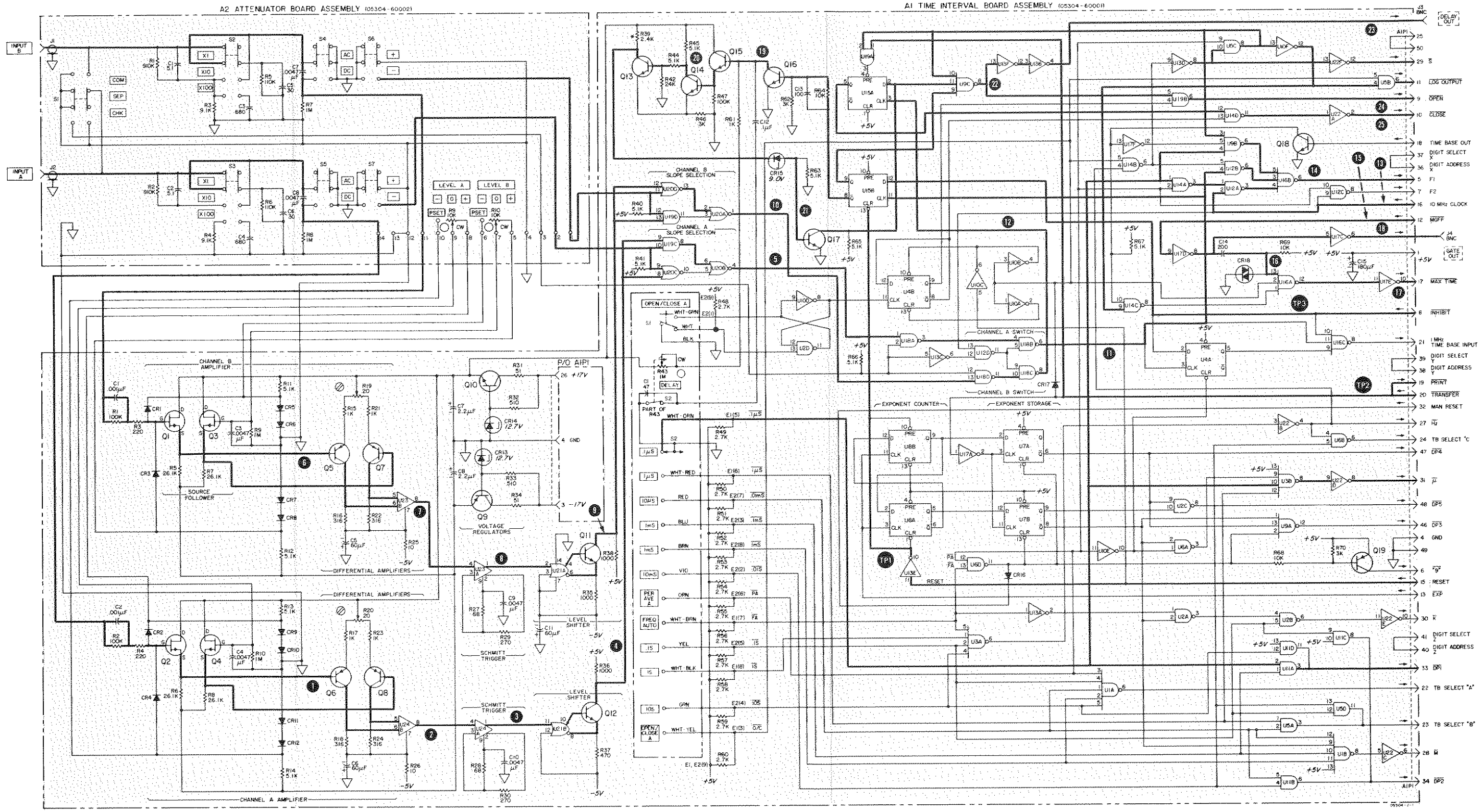


Figure 9D-5-4. Time Interval Troubleshooting Diagram

TIME INTERVAL TROUBLESHOOTIN
I

(See I

OPEN/CLOSE MODE

5304A Controls:

Channel A, SEP, X1, DC, +, PSET OPEN/CLOSE A. Press RESET, then OPEN/CLOSE; display should be accumulating at a 10 Hz rate.

INPUT:

651B set to 10 Hz, 100 mV rms/50Ω.

Oscilloscope:

HP 180A, HP 1801A Vert Amp, HP 1821A T.B. through a 10:1 probe.

Settings:

AC coupled (except as noted).
NORM sweep mode.
+ slope (except as noted)
AC (except as noted)
Channel A

5300A Sample Rate ccw out of OFF (except as noted).

5304A: OPEN/CLOSE Mode

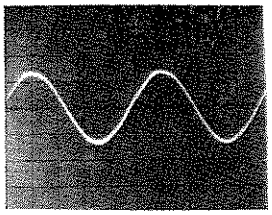
TP1 H. Goes Low when OPEN/CLOSE switch is pressed. Reamains Low if this switch is held depressed.

TP2 L. Goes High when RESET is pressed. Remains High if this switch is held depressed.

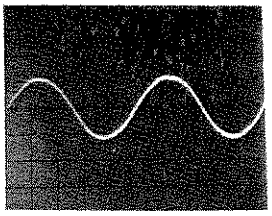
TP3 L

TP4 L. Goes High when OPEN/CLOSE is pressed to stop accumulation or when RESET is pressed during accumulation.

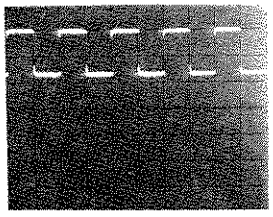
TP5 H. Goes Low when OPEN/CLOSE is pressed to stop accumulation or when RESET is pressed during accumulation.



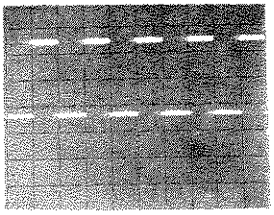
❶ .01 V/cm
20 msec/cm



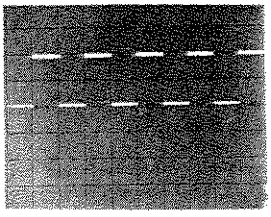
❷ .02 V/cm
20 msec/cm



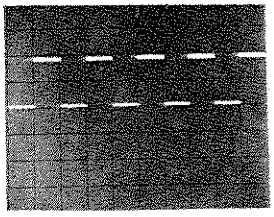
❸ .05 V/cm
50 msec/cm
dc coupled



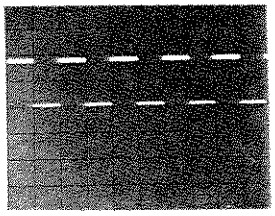
❹ .2 V/cm
50 msec
dc coupled



❺ .2 V/cm
50 msec/cm
dc coupled



❻ .2 V/cm
50 msec/cm
dc coupled



❼ .2 V/cm
50 msec/cm
dc coupled

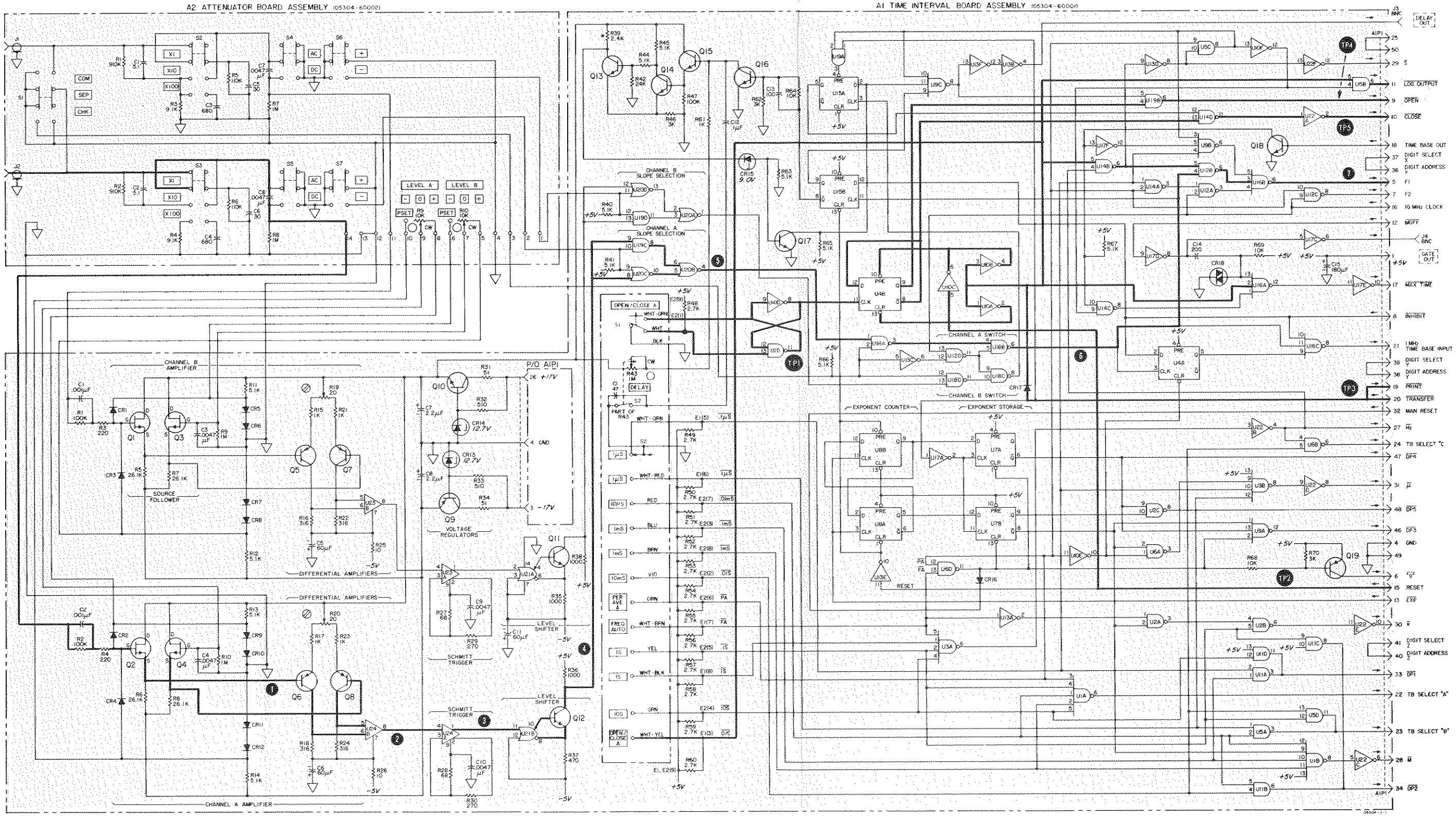


Figure 9D-5-5. Open/Close Troubleshooting Diagram

OPEN/CLOSE TROUBLESHOOT
(See

CHECK MODE

5304A Controls:

COM/SEP/CHK to CHK; "Function" to AUTO

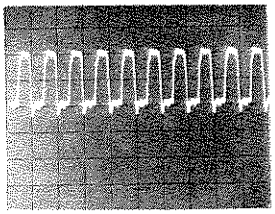
5300A Display should be 10.0000 MHz C ±1 count.

Oscilloscope:

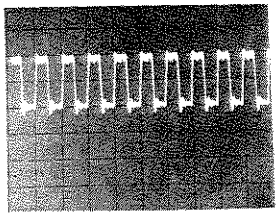
HP 180A, HP 1801A Vert Amp, HP 1821A T.B. through a 10:1 probe

Settings:

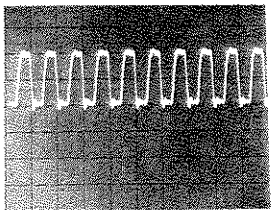
AC coupled (except as noted).
NORM sweep mode.
+ Slope (except as noted).
AC (except as noted).
Channel A.



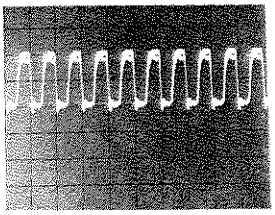
❶ .2 V/cm
.1 μsec/cm
dc coupled



❷ .2 V/cm
.1 μsec/cm
dc coupled



❸ .2 V/cm
.1 μsec/cm
dc coupled



❹ .2 V/cm
.1 μsec/cm
dc coupled

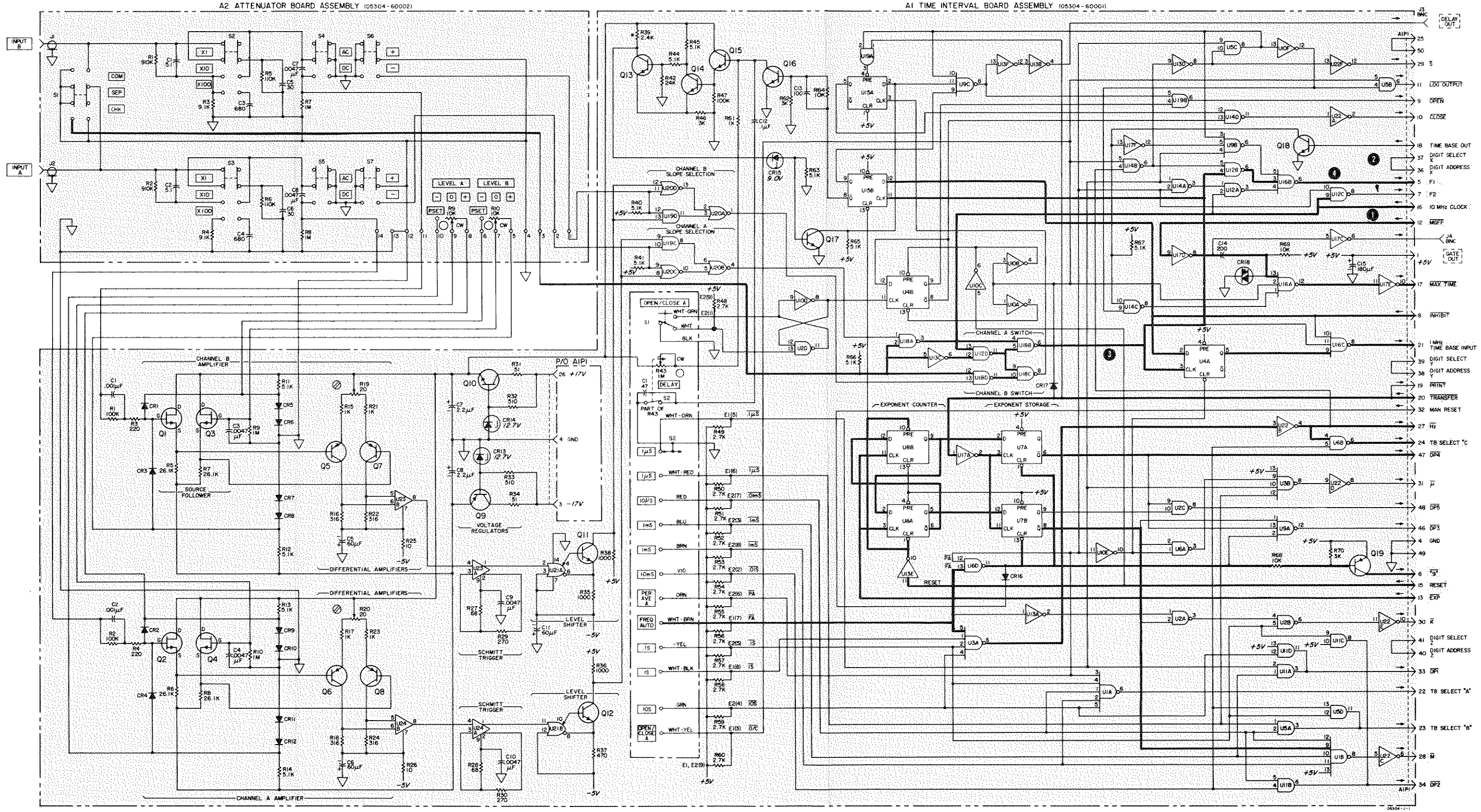


Figure 9D-5-6. Check Troubleshooting Diagram

F
CHECK TROUBLESHOOTIN
(See P

Table 9D-5-1. In-Cabinet Performance Checks

1. CHK mode and Time Interval Holdoff.
   a. Set 5300A OSC switch to INT.
   b. Mate 5300A to 5304A and ensure side casting latches at rear of 5300A are latched.
   c. Connect ac power to 5300A ac receptacle.
   d. Turn ac power "on" with 5300A SAMPLE RATE slightly cw out of OFF.
   e. Set COM-SEP-CHK to CHK; "Function" switch to FREQ A, AUTO. Display should be 10.0000 MHz ±1 count.
   f. Set "Function switch to T. I. A to B, .1 μsec. Press 5300A RESET switch; the 5300A display should be about .2 μsec (200 nsec residual holdoff). It may also be .0 μsec.
   g. Set the DELAY slightly cw out of the detent position. Display should be approximately 100 μsec.
   h. Adjust the DELAY control cw until maximum setting is reached. Display should be about * 00000.0 μs (* = OVERFLOW) (100,000.0 μsec).
   i. Repeat steps g and h for the following ranges; display should be as listed.

T. I. A to B	Approximate 5300A Display with DELAY control: ccw out of Detent	max. cw
1 μsec	000100 μsec	100000 μsec
10 μsec	0000.10 MS	0100.00 MS
1 ms	00000.0 MS	00100.0 MS
1 ms	000000 MS	000100 MS
10 ms	0000.00 S	0000.10 S

2. FREQ A Mode.

   RANGE: dc coupled: 0 to 10 MHz.

   ac coupled: 100 Hz to 10 MHz.

   Sensitivity as in Table 9D-1-1.

   Obtain following test Equipment:

   HP 651B Test Oscillator
   HP 11048B 50-Ohm Feed-Thru Termination

   Table 5-1 in the 5300A portion of the manual and Table 9D-5-1 lists equipment used; equipment with equivalent characteristics may be used.

   a. Connect 651B 50-Ohm OUTPUT through the 50-Ohm feed-thru to 5304A "A INPUT" connector. Set 5304A "Function" switch to FREQ A, AUTO; set COM-SEP-CHK to SEP, ATTEN to X1, AC-DC to AC, SLOPE to +, LEVEL to PSET or adjusted until a stable count is displayed.
   b. Set 651B to frequencies and output levels listed below: Display should be as listed.

3. FREQ A Mode, Pulse Measurements.

   RANGE: dc coupled: 0 to 10 MHz

   Sensitivity as in Table 9D-1-1.

   Pulse Width: 40 nsec minimum

   Obtain the following test equipment:

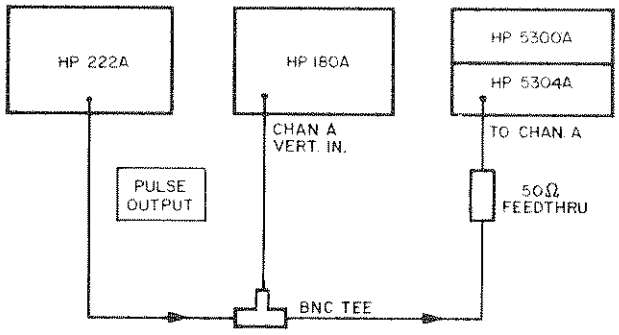
   HP Model 222A Pulse Generator
   HP Model 11048B 50-ohm Feed-thru Termination
   HP Model 180A Oscilloscope
   BNC Tee Connector

   a. Connect equipment as in Figure A.

651B OUTPUT mV rms	651B FREQ Hz Approximate	"Function" (sec)	Approximate Display ±1 Count ± Accuracy of source
25	10 Hz	10	00010.0 Hz
25	10 kHz	10	10000.0 Hz
25	100 kHz	1	100000 Hz
25	1 MHz	.1	1000.00 kHz
50	10 MHz	AUTO	10.0000 MHz

Table 9D-5-1. In-Cabinet Performance Checks (Continued)

Figure A



b. Set 222A for "+" PULSE POLARITY; 40 nsec pulse width; 150 mV p-p as monitored on oscilloscope.

c. Monitor 222A pulse output with oscilloscope and set REP RATE for 10 Hz.

d. Set 5304A Channel A controls as follows:

ATTEN switch to X1
AC-DC to DC
SLOPE to +.
LEVEL to PSET or adjust until a stable count is displayed.

e. 5300A display should be approximately 10 Hz.

f. Repeat step c with 222A repetition rates of 10 kHz, 100 kHz, 1 MHz and 10 MHz. The 5300A display should be the same as the 222A repetition rate setting.

g. Set 222A PULSE POLARITY to "-". Set 5304A Channel A SLOPE to -. Repeat steps b through f.

4. PER AVG A Mode.

RANGE: 10 Hz (.1 sec) to 1 MHz (1 μsec).

Obtain the following test equipment:

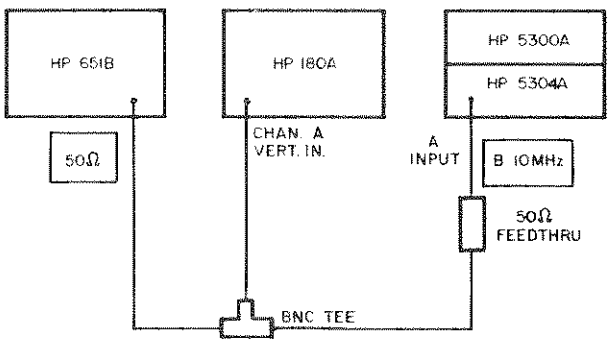
HP Model 651B Test Oscillator.
HP Model 11048B 50 OHM Feed-thru Termination.

a. Connect equipment as shown in Figure B.

b. Set 5304A Channel A controls as follows:

1. "Function" switch to PER AVG A.
2. ATTEN to X1.
3. AC-DC to AC.

Figure B



4. SLOPE to +.
5. LEVEL to PSET or adjusted until a stable display is obtained.

c. Monitor the oscilloscope and set 651B controls for 10 Hz, 100 mV rms output.

d. Display should be approximately * 00.0000 MS, C (* = OVERFLOW) (100 msec).

e. Monitor the oscilloscope and set 651B for the following frequencies; display should be as listed.

651B	5300A/5304A
10 kHz	100.000 μs C
100 kHz	10.0000 μs C
1 MHz	01.0000 μs C

NOTE

Periods averaged are automatically selected to provide maximum resolution.

5. T. I. A to B (Time Interval) Mode.

RANGE: 500 nsec to 10,000 seconds.

Obtain the following test equipment:

HP Model 222A Pulse Generator (2 required).

HP Model 11048B 50-Ohm Feed-thru Termination (2 required).

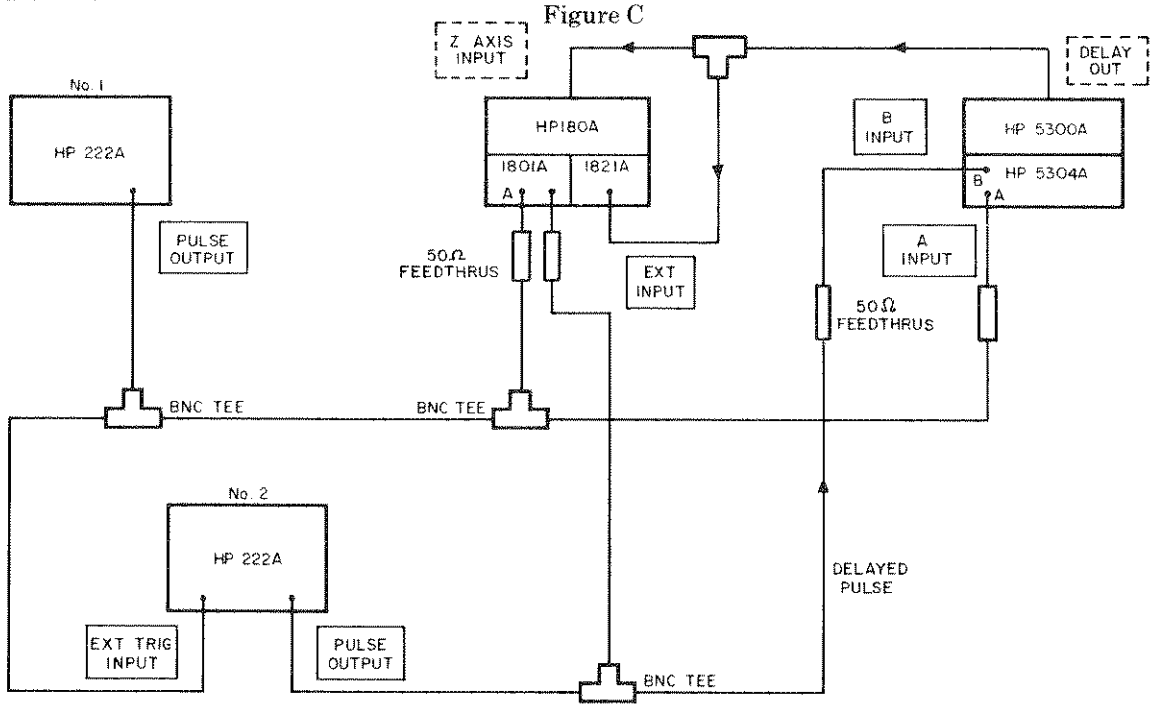
HP Model 180A Oscilloscope.

BNC Tee Connectors, (3 required).

a. Connect equipment as shown in Figure C.

Table 9D-5-1. In-Cabinet Performance Checks (Continued)

Figure C



b. While monitoring generator No. 1 output with oscilloscope, set No. 1 generator controls as follows:

   1. REP RATE to 1k-10k with adjustment centered.
   2. PULSE WIDTH for .2 μsec pulse at 2 V amplitude.
   3. PULSE POLARITY to +.

c. While monitoring generator No.2 output with oscilloscope, set No. 2 generator controls as follows:

   1. REP RATE to MAN/EXT +.
   2. PULSE POLARITY to +.
   3. PULSE WIDTH for .2 μsec pulse at 2 V amplitude.
   4. PULSE DELAY for .5 μsec.

d. Set Oscilloscope DISPLAY control to A + B to monitor No.2 pulse position.

e. Set 5304A control as follows:

   1. ATTEN (both channels) to X1.
   2. AC-DC (both channels) to DC.
   3. SLOPE (both channels) to +.
   4. LEVEL (both channels to PSET.
   5. COM-SEP-CHK to SEP.

f. 5304A should display 00000.5 μsec; verify time interval with oscilloscope.

g. While monitoring oscilloscope, adjust No. 2 generator PULSE DELAY for time intervals from .5 μsec to 150 μsec. 5300A Display should be the same as oscilloscope display.

h. Set No. 1 generator REP RATE to 100-1k and adjustment centered.

i. While monitoring oscilloscope, adjust No. 2 generator PULSE DELAY for time intervals from 150 μsec to 2000 μsec. 5300A display should be the same as oscilloscope display.

j. Set No. 1 generator REP RATE to 10-100 and adjustment full ccw.

k. While monitoring oscilloscope, adjust No. 2 generator PULSE DELAY for time intervals from 2000 μsec to 6000 μsec. 5300A display and oscilloscope display should indicate the same time intervals.

NOTE

Measurement resolution may be adjusted from .1 μsec to 1 msec with the T.I. A to B switch.

Table 9D-5-1. In-Cabinet Perfomrance Checks (Continued)

6. Totalizing (OPEN/CLOSE A) Measurements.

Obtain the following test equipment:

HP Model 651B Test Oscillator.

HP Model 11048B 50-Ohm Feed-thru Termination.

a. Connect 651B 50-Ohm output, set to 10 Hz at 100 mV rms, to 5304A Channel A INPUT connector.

b. Set Channel A ATTEN switch to X100, AC-DC to AC; SLOPE to + and LEVEL to PSET.

c. Set "Function" switch to OPEN/CLOSE A.

d. Instrument gate is controlled by operator when OPEN/CLOSE A pushbutton is pressed.

e. Press OPEN/CLOSE A switch; 5300A C lamp will turn on; adjust Channel A ATTEN to X1; 5300A display should accumulate.

f. To stop 5300A from accumulating, press OPEN/CLOSE A. To continue accumulation from the number displayed press OPEN/CLOSE A, otherwise press RESET to clear display.

PERFORMANCE CHECK TEST CARD

Hewlett-Packard Model 5300A/5304A
TIMER/COUNTER

Test Performed by _____

Serial No. _____ - _____

Date _____

Description	Check
1. CHECK Mode and Time Interval Holdoff. Display is 10 MHz ±1 Count. Hold off as in Table 9D-5-1, item 1, step i.	☐
2. FREQ A Mode. 0 to 10 MHz dc coupled. 100 Hz to 10 MHz ac coupled.	☐
3. FREQ A Pulse Measurement Mode. Channel A; 0 to 10 MHz 40 nsec minimum.	☐
4. PER AVG A Mode. 10 Hz (.1 sec) to 1 MHz (1 μsec).	☐
5. TIME INTERVAL Mode 500 nsec to 10,000 seconds. (tested to 6000 μsec).	☐
6. Totalizing (OPEN/CLOSE A). Controlled accumulation.	☐

SECTION IX D
5304A TIMER/COUNTER

SUBSECTION VI
REPLACEABLE PARTS

9D-6-1. INTRODUCTION

9D-6-2. This subsection contains information for ordering replacement parts. Table 9D-6-1 lists parts used in the HP 5304A.

9D-6-3. ORDERING INFORMATION

9D-6-4. To obtain replacement parts address order or inquiry to your local Hewlett-Packard Sales and Service Office (see lists in Section VI, 5300A Manual for addresses). Identify parts by their Hewlett-Packard part number. To obtain a part that is not listed, include:

a. Instrument model number.

b. Instrument serial number.

c. Description of the part.

d. Function and location of the part.

REFERENCE DESIGNATORS

A	assembly	F	fuse	MP	mechanical part	U	integrated circuit
B	motor	FL	filter	P	plug	V	vacuum, tube, neon bulb, photocell, etc.
BT	battery	IC	integrated circuit	Q	transistor		
C	capacitor	J	jack	R	resistor	VR	voltage regulator
CP	coupler	K	relay	RT	thermistor	W	cable
CR	diode	L	inductor	S	switch	X	socket
DL	delay line	LS	loud speaker	T	transformer	Y	crystal
DS	device signaling (lamp)	M	meter	TB	terminal board	Z	tuned cavity, network
E	misc electronic part	MK	microphone	TP	test point		

ABBREVIATIONS

A	amperes	H	henries	N/O	normally open	RMO	rack mount only
AFC	automatic frequency control	HDW	hardware	NOM	nominal	RMS	root-mean square
AMPL	amplifier	HEX	hexagonal	NPO	negative positive zero (zero temperature coefficient)	RWV	reverse working voltage
BFO	beat frequency oscillator	HG	mercury			S-B	slow-blow
BE CU	beryllium copper	HR	hour(s)			SCR	screw
BH	binder head	HZ	hertz	NPN	negative-positive-negative	SE	selenium
BP	bandpass	IF	intermediate freq	NRFR	not recommended for field replacement	SECT	section(s)
BRS	brass	IMPG	impregnated			SEMICON	semiconductor
BWO	backward wave oscillator	INCD	incandescent	NSR	not separately replaceable	SI	silicon
		INCL	include(s)			SIL	silver
CCW	counter-clockwise	INS	insulation(ed)	OBD	order by description	SL	slide
CER	ceramic	INT	internal	OH	oval head	SPG	spring
CMO	cabinet mount only	K	kilo = 1000	OX	oxide	SPL	special
COEF	coefficient			P	peak	SST	stainless steel
COM	common	LH	left hand	PC	printed circuit	SR	split ring
COMP	composition	LIN	linear taper	PF	picofarads = 10^{-12} farads	STL	steel
COMPL	complete	LK WASH	lock washer			TA	tantalum
CONN	connector	LOG	logarithmic taper	PH BRZ	phosphor bronze	TD	time delay
CP	cadmium plate	LPF	low pass filter	PHL	Phillips	TGI	toggle
CRT	cathode-ray tube	M	milli = 10^{-3}	PIV	peak inverse voltage	THD	thread
CW	clockwise	MEG	meg = 10^{6}	PNP	positive-negative-positive	TI	titanium
DEPC	deposited carbon	MET FLM	metal film	P/O	part of	TOL	tolerance
DR	drive	MET OX	metallic oxide	POLY	polystyrene	TRIM	trimmer
ELECT	electrolytic	MFR	manufacturer	PORC	porcelain	TWT	traveling wave tube
ENCAP	encapsulated	MHZ	mega hertz	POS	position(s)	U	micro = 10^{-6}
EXT	external	MINAT	miniature	POT	potentiometer	VAR	variable
F	farads	MOM	momentary	PP	peak-to-peak	VDCW	dc working volts
FH	flat head	MOS	metal ozide substrate	PT	point	W	with
FIL H	fillister head	MTG	mounting	PWV	peak working voltage	W	watts
FXD	fixed	MY	"mylar"	RECT	rectifier	WIV	working inverse voltage
G	giga (10^{9})	N	nano (10^{-9})	RF	radio frequency	WW	wirewound
GE	germanium	N/C	normally closed	RH	round head or right hand	W/O	without
GL	glass	NE	neon				
GRD	ground(ed)	NI PL	nickel plate				

01194-14

Table 9D-6-1. Replace Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	05304-60001	1	BOARD ASSY: TIME INTERVAL (Not available for field replacement or sale) (Includes A2, 05304-60002)	28480	05304-60001
A1C1	0150-0050	2	C:FXD CER 1000 PF +80-20% 1000VDCW	56289	C067B102E102Z S26-CDH
A1C2	0150-0050		C:FXD CER 1000 PF +80-20% 1000VDCW	56289	C067B102E102Z S26-CDH
A1C3	0150-0075	6	C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z
A1C4	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z
A1C5	0180-0106	3	C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A1C6	0180-0106		C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A1C7	0180-0197	2	C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2-DYS
A1C8	0180-0197		C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2-DYS
A1C9	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z
A1C10	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z
A1C11	0180-0106		C:FXD ELECT 60 UF 20% 6VDCW	28480	0180-0106
A1C12	0160-0168	1	C:FXD MY 0.1 UF 10% 200VDCW	56289	192P10492-PTS
A1C13	0160-2204	1	C:FXD MICA 100PF 5%	72136	RDM15F101J3C
A1C14	0140-0198	19	C:FXD MICA 200 PF 5%	72136	RDM15F201J3C
A1C15	0180-1702	1	C:FXD ELECT 180 UF 20% 6VDCW	56289	150D187X0006R2-DYS
A1CR1	1901-0376	4	DIODE:SILICON 35V	28480	1901-0376
A1CR2	1901-0376		DIODE:SILICON 35V	28480	1901-0376
A1CR3	1901-0376		DIODE:SILICON 35V	28480	1901-0376
A1CR4	1901-0376		DIODE:SILICON 35V	28480	1901-0376
A1CR5	1901-0040	10	DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR6	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR7	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR8	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR9	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR10	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR11	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR12	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR13	1902-0031	2	DIODE BREAKDOWN:12.7V 5%	28480	1902-0031
A1CR14	1902-0031		DIODE BREAKDOWN:12.7V 5%	28480	1902-0031
A1CR15	1902-3149	1	DIODE BREAKDOWN:9.09V 5%	28480	1902-3149
A1CR16	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR17	1901-0040		DIODE:SILICON 30MA 30WV	07263	FDG1088
A1CR18	1901-0460	1	DIODE:SILICON 3-JUNCTION STABISTOR	03508	STB523
A1E1	1810-0041	2	R:NETWORK,8 RES. 2.7K OHM 5%	28480	1810-0041
A1E2	1810-0041		R:NETWORK,8 RES. 2.7K OHM 5%	28480	1810-0041
A1P1	1251-2756	1	CONNECTOR:R & P, 50 CONTACT	74868	57-20500-31
A1Q1	05304-80001	2	TRANSISTOR:FET MATCHED	28480	05304-80001
A1Q2	05304-80001		TRANSISTOR:FET MATCHED	28480	05304-80001
A1Q3			(PART OF A1Q1)		
A1Q4			(PART OF A1Q2)		
A1Q5	1853-0036	6	TSTR:SI PNP	80131	2N3906
A1Q6	1853-0036		TSTR:SI PNP	80131	2N3906
A1Q7	1853-0036		TSTR:SI PNP	80131	2N3906
A1Q8	1853-0036		TSTR:SI PNP	80131	2N3906
A1Q9	1853-0036	1	TSTR: SI PNP	80131	2N3906
A1Q10	1854-0246		TSTR: SI NPN	80131	2N3643
A1Q11	1854-0094	4	TSTR:SI NPN	80131	2N3646
A1Q12	1854-0094		TSTR:SI NPN	80131	2N3646
A1Q13	1854-0071	4	TSTR:SI NPN(SELECTED FROM 2N3704)	28480	1854-0071
A1Q14	1854-0071		TSTR:SI NPN(SELECTED FROM 2N3704)	28480	1854-0071
A1Q15	1854-0071		TSTR:SI NPN(SELECTED FROM 2N3704)	28480	1854-0071
A1Q16	1854-0071		TSTR:SI NPN(SELECTED FROM 2N3704)	28480	1854-0071
A1Q17	1854-0094		TSTR:SI NPN	80131	2N3646
A1Q18	1854-0094		TSTR:SI NPN	80131	2N3646
A1Q19	1853-0036		TSTR:SI PNP	80131	2N3906
A1R1	0683-1045	3	R:FXD COMP 100K OHMS 5% 1/4W	01121	CB 1045
A1R2	0683-1045		R:FXD COMP 100K OHMS 5% 1/4W	01121	CB 1045
A1R3	0683-2215	2	R:FXD COMP 220 OHM 5% 1/4W	01121	CB 2215
A1R4	0683-2215		R:FXD COMP 220 OHM 5% 1/4W	01121	CB 2215
A1R5	0698-3159	4	R:FXD MET FLM 26.1K OHM 1% 1/8W	28480	0698-3159
A1R6	0698-3159		R:FXD MET FLM 26.1K OHM 1% 1/8W	28480	0698-3159
A1R7	0698-3159		R:FXD MET FLM 26.1K OHM 1% 1/8W	28480	0698-3159
A1R8	0698-3159		R:FXD MET FLM 26.1K OHM 1% 1/8W	28480	0698-3159
A1R9	0683-1055	5	R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A1R10	0683-1055		R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A1R11	0683-5125	12	R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R12	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R13	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R14	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R15	0757-0280	4	R:FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A1R16	0698-3444	4	R:FXD MET FLM 316 OHM 1% 1/8W	28480	0698-3444
A1R17	0757-0280		R:FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A1R18	0698-3444		R:FXD MET FLM 316 OHM 1% 1/8W	28480	0698-3444
A1R19	2100-1768	2	R:VAR WW 20 OHM 5% TYPE H 1W	28480	2100-1768

See introduction to this section for ordering information

Table 9D-6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R20	2100-1768		P:VAR WW 20 OHM 5% TYPE H 1W	28480	2100-1768
A1R21	0757-0280		R:FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A1R22	0698-3444		R:FXD MET FLM 316 OHM 1% 1/8W	28480	0698-3444
A1R23	0757-0280		R:FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A1R24	0698-3444		R:FXD MET FLM 316 OHM 1% 1/8W	28480	0698-3444
A1R25	0683-1005	2	R:FXD COMP 10 OHM 5% 1/4W	01121	CB 1005
A1R26	0683-1005		R:FXD COMP 10 OHM 5% 1/4W	01121	CB 1005
A1R27	0683-6805	2	R:FXD COMP 68 OHM 5% 1/4W	01121	CB 6805
A1R28	0683-6805		R:FXD COMP 68 OHM 5% 1/4W	01121	CB 6805
A1R29	0683-2715	2	R:FXD COMP 270 OHM 5% 1/4W	01121	CB 2715
A1R30	0683-2715		R:FXD COMP 270 OHM 5% 1/4W	01121	CB 2715
A1R31	0683-5105	2	R:FXD COMP 51 OHM 5% 1/4W	01121	CB 5105
A1R32	0683-5115	2	R:FXD COMP 510 OHM 5% 1/4W	01121	CB 5115
A1R33	0683-5115		R:FXD COMP 510 OHM 5% 1/4W	01121	CB 5115
A1R34	0683-5105		R:FXD COMP 51 OHM 5% 1/4W	01121	CB 5105
A1R35	0683-4715	2	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715
A1R36	0683-1025		R:FXD COMP 1000 OHM 5% 1/4W	01121	CB 1025
A1R37	0683-4715	3	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715
A1R38	0683-1025		R:FXD COMP 1000 OHM 5% 1/4W	01121	CB 1025
A1R39	0683-2425	1	R:FXD COMP 2400 OHM 5% 1/4W FACTORY SELECT	01121	CB 2425
A1R40	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R41	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R42	0683-2435	1	R:FXD COMP 24K OHM 5% 1/4W	01121	CB 2435
A1R43	0683-1055		R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A1R44	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R45	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R46	0683-3025	3	R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A1R47	0683-1045		R:FXD COMP 100K OHMS 5% 1/4W	01121	CB 1045
A1R48, A1R60 PART OF E1, E2	1801-0041		R:FXD 2.7K PART OF E1, E2	28480	1801-0041
A1R61	0683-1025		R:FXD COMP 1000 OHM 5% 1/4W	01121	CB 1025
A1R62	0683-3025		R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A1R63	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R64	0683-1035	3	R:FXD COMP 10K OHM 5% 1/4W	01121	CB 1035
A1R65	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R66	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R67	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R68	0683-1035		R:FXD COMP 10K OHM 5% 1/4W	01121	CB 1035
A1R69	0683-1035		R:FXD COMP 10K OHM 5% 1/4W	01121	CB 1035
A1R70	0683-3025		R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A1U1	1820-0441	1	IC:DUAL 5-INPUT NAND GATE	04713	SC8171PK
A1U2	1820-0094	2	IC:DTL QUAD 2-INPT GATE	28480	1820-0094
A1U3	1820-0069	1	IC:TTL DUAL 4-INPT POS NAND GATE	01295	SN4344
A1U4	1820-0077	4	IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U5	1820-0273	2	IC:DTL QUAD 2-INPT AND GATE	28480	1820-0273
A1U6	1820-0094		IC:DTL QUAD 2-INPT GATE	28480	1820-0094
A1U7	1820-0077		IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U8	1820-0077		IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U9	1820-0068	2	IC:TTL TRIPLE 3-INPUT POS NAND GATE	12040	SN7410N
A1U10	1820-0307	1	IC:DIGITAL DTL HEX INVERTER	28480	1820-0307
A1U11	1820-0273		IC:DTL QUAD 2-INPT AND GATE	28480	1820-0273
A1U12	1820-0370	1	IC:TTL QUAD 2-INPT NAND GATE	01295	SN5478
A1U13	1820-0174	2	INTEGRATED CIRCUIT:TTL HEX INVERTER	01295	SN8199
A1U14	1820-0054	2	IC:TTL QUAD 2-INPUT NAND GATE	01295	SN4342
A1U15	1820-0077		IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U16	1820-0068		IC:TTL TRIPLE 3-INPUT POS NAND GATE	12040	SN7410N
A1U17	1820-0174		INTEGRATED CIRCUIT:TTL HEX INVERTER	01295	SN8199
A1U18	1820-0054		IC:TTL QUAD 2-INPUT NAND GATE	01295	SN4342
A1U19	1820-0511	1	IC:TTL QUAD 2-INPT & GATE	01295	SN2C572
A1U20	1820-0328	1	IC:TTL QUAD 2-INPT NOR GATE	01295	SN4467
A1U21	1820-0578	1	IC:DIGITAL DUAL 2-INPT OR/NOR GATE	04713	SC7383PK
A1U22	1820-0577	1	IC:DIGITAL TTL HEX INVERTER	01295	SN22729
A1U23	1820-0253	2	INTEGRATED CIRCUIT:DIGITAL ECL DUAL	04713	MC1035P
A1U24	1820-0253		INTEGRATED CIRCUIT:DIGITAL ECL DUAL	04713	MC1035P
A2	05304-60003	1	BOARD ASSY:ATTENUATOR	28480	05304-60003
A2XA Misc.	05300-20007	1	PIN:CONNECTOR GROUP PC. Contains 36 pc right angle CONNECTORS. Only 14 are used.	28480	05300-20007
A2C1	0160-2250	2	C:FXD CER 5.1 PF 500VDCW	72982	301-000-COH0-519E
A2C2	0160-2250		C:FXD CER 5.1 PF 500VDCW	72982	301-000-COH0-519E
A2C3	0140-0208	2	C:FXD MICA 680 PF 5%	72136	RDM15F681J3C
A2C4	0140-0208		C:FXD MICA 680 PF 5%	72136	RDM15F681J3C
A2C5	0160-2199	2	C:FXD MICA 30 PF 5% 300VDCW	28480	0160-2199
A2C6	0160-2199		C:FXD MICA 30 PF 5% 300VDCW	28480	0160-2199
A2C7	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z
A2C8	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z

See introduction to this section for ordering information

Table 9D-6-1. Replaceable Parts (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2J1	1250-1163	2	CONNECTOR:RF BNC INPUT	28480	1250-1163
A2J2	1250-1163		CONNECTOR:RF BNC INPUT	28480	1250-1163
A2R1	0683-9145	2	R:FXD COMP 910K OHM 5% 1/4W	01121	CB 9145
A2R2	0683-9145		R:FXD COMP 910K OHM 5% 1/4W	01121	CB 9145
A2R3	0683-9125	2	R:FXD COMP 9100 OHM 5% 1/4W	01121	CB 9125
A2R4	0683-9125		R:FXD COMP 9100 OHM 5% 1/4W	01121	CB 9125
A2R5	0698-3576	2	R:FXD COMP 110K OHM 5% 1/4W	28480	0698-3576
A2R6	0698-3576		R:FXD COMP 110K OHM 5% 1/4W	28480	0698-3576
A2R7	0683-1055		R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A2R8	0683-1055		R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A2R9	2100-3228	2	R:VAR CERMET 10K OHM 10% LIN	28480	2100-3228
A2R10	2100-3228		R:VAR CERMET 10K OHM 10% LIN	28480	2100-3228
A2S2	3101-1598		SWITCH:SLIDE DP3T 0.5A 125V AC/DC	28480	3101-1598
A2S3	3101-1598		SWITCH:SLIDE DP3T 0.5A 125V AC/DC	28480	3101-1598
A2S4	3101-1596	4	SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
A2S5	3101-1596		SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
A2S6	3101-1596		SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
A2S7	3101-1596		SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
			CHASSIS PARTS		
J1	1250-0083	2	CONNECTOR:BNC	02660	31-221-1020
C1	0160-0182	1	C:FXD 47 pf, 5%, 300V	14655	
J2	1250-0083		CONNECTOR:BNC	02660	31-221-1020
R43	2100-3078	1	R:VAR COMP 1 MEGOHM 20% (PART OF S2)	28480	2100-3078
S1	3101-1159	1	SWITCH:PUSHBUTTON SPDT	82389	10S-1051
S2	3100-2922	1	SWITCH:ROTARY	28480	3100-2922
S3			(PART OF R43)		
W1	05304-60004	1	CABLE ASSY	28480	05304-60004
			MISCELLANEOUS PARTS		
	0370-1005	2	KNOB:JADE GREY	28480	0370-1005
	0370-1100	1	KNOB:JADE GREY	28480	0370-1100
	0370-2102	1	KNOB	28480	0370-2102
	05245-2016	1	COUPLER	28480	05245-2016
	05300-40003	4	SUPPORT:BOARD	28480	05300-40003
	05300-40004	4	GUIDE:SLIDE	28480	05300-40004
	05301-20005	1	STAND:TILT	28480	05301-20005
	05300-80004	1	COVER: PLASTIC DUST PROTECTION	28480	05300-80004
	05304-00001	1	PANEL:FRONT	28480	05304-00001
	05304-00004	1	PANEL:REAR	28480	05304-00004
	0624-0208	8	SCREW: SELF TAP, CAD. PLATE, 6/32 x 1/2"	28480	0624-0208
	05300-20010	1	CASE:ALUMINIUM, CAST	28480	05300-20010
	5040-7032	1	FOOT: REAR	28480	5040-7032

See introduction to this section for ordering information

Table 9D-6-1. Manufacturers Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
01121	ALLEN BRADLEY CO.	MILWAUKEE, WIS.	53204
01295	TEXAS INSTRUMENTS INC. SEMICONDUCTOR COMPONENTS DIV.	DALLAS, TEX.	75231
02660	AMPHENOL CORP.	BROADVIEW, ILL.	60153
03508	G.E. CO. SEMICONDUCTOR PROD. DEPT.	SYRACUSE, N.Y.	13201
04713	MOTOROLA SEMICONDUCTOR PROD.INC.	PHOENIX, ARIZ.	85008
07263	FAIRCHILD CAMERA & INST. CORP. SEMICONDUCTOR DIV.	MOUNTAIN VIEW, CALIF.	94040
12040	NATIONAL SEMICONDUCTOR CORP.	DANBURY, CONN.	06810
28480	HEWLETT-PACKARD COMPANY	PALO ALTO, CALIF.	94304
56289	SPRAGUE ELECTRIC CO.	N. ADAMS, MASS.	01247
72136	ELECTRO MOTIVE MFG. CO. INC.	WILLIMANTIC, CONN.	06226
72982	ERIE TECHNOLOGICAL PROD. INC.	ERIE, PA.	16512
74868	AMPHENOL CORP. RF DIV.	DANBURY, CONN	06810
79727	CONTINENTAL-WIRT ELECTRONICS CORP.	PHILADELPHIA, PA.	19144
80131	ELECTRONIC INDUSTRIES ASSOCIATION	WASHINGTON D.C.	20006
82389	SWITCHCRAFT INC.	CHICAGO, ILL.	60630
14655	CORNELL-DUBILIER	NEWARK, N.J.	

SECTION IX D
5304A TIMER/COUNTER

SUBSECTION VII
MANUAL CHANGES AND OPTIONS

9D-7-1. MANUAL CHANGES

9D-7-2. Section IX D applies directly to Models 5304A Timer/Counter having serial prefix number 1212A00467.

9D-7-3. NEWER INSTRUMENTS

9D-7-4. As changes are made, newer instruments may have serial prefix numbers not listed in Section IX D. The manuals for these instruments will be supplied with "manual changes" pages containing the required information; replace the affected pages with the "replacement manual changes" pages. Contact the nearest Hewlett-Packard Sales and Service Office for information if this sheet is missing.

9D-7-5. OLDER INSTRUMENTS

9D-7-6. Changes for 5304A instruments with serial numbers 1116A00466 and below are listed as replacement pages in Table 9D-7-1, 7-2, 7-3, and Figure 9D-7-1.

To back date the manual, do the following:

Replace the 5304A Title Page with the replacement page containing Tables 9D-7-1 and 7-2. Replace page 9D-6-3 and 9D-6-4 with replacement page containing Table 9D-7-3 and 7-4. Replace page 9D-8-5 with replacement page containing Figure 9D-7-1.

9D-7-7. OPTIONS

9D-7-8. No options at time of printing.

Table 9D-7-1. 5304A Section IX D Timer/Counter Title Page

SECTION IX D
TIMER/COUNTER
5304A

SERIAL PREFIX: 1116A

This section applies directly to HP Model 5304A, Timer/Counters having serial prefix number 1116A, and must be inserted into the 5300A Measuring System Manual.

NEWER INSTRUMENTS

This Section with enclosed "Manual Changes Sheet(s)" applies directly to HP Model 5304A Timer/Counters having prefix numbers above 1116A.

OLDER INSTRUMENTS

Changes required to back-date this Section for older instruments are in Section IX D, Subsection VII.

Table 9D-7-2. Table of Contents

TABLE OF CONTENTS

Table 9D-7-3. Replaceable Parts

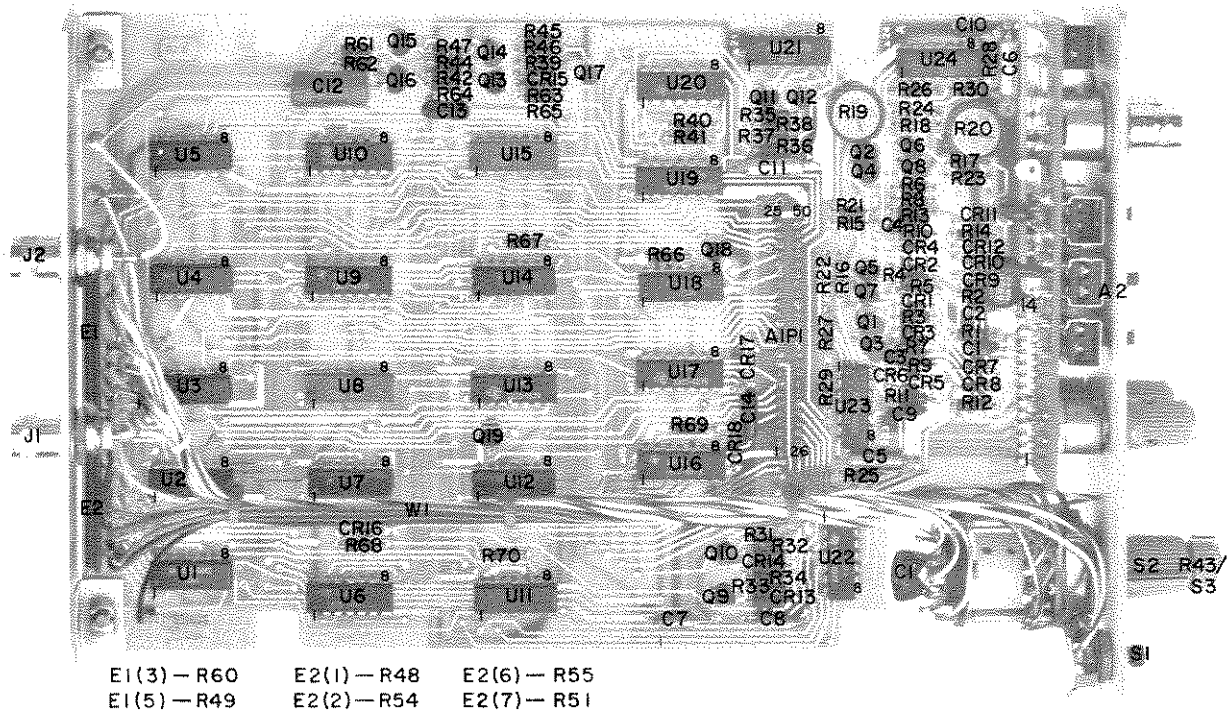
Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R20	2100-1768		P:VAR WW 20 OHM 5% TYPE H 1W	28480	2100-1768
A1R21	0757-0280		R:FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A1R22	0698-3444		R:FXD MET FLM 316 OHM 1% 1/8W	28480	0698-3444
A1R23	0757-0280		R:FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A1R24	0698-3444		R:FXD MET FLM 316 OHM 1% 1/8W	28480	0698-3444
A1R25	0683-1005	2	R:FXD COMP 10 OHM 5% 1/4W	01121	CB 1005
A1R26	0683-1005		R:FXD COMP 10 OHM 5% 1/4W	01121	CB 1005
A1R27	0683-6805	2	R:FXD COMP 68 OHM 5% 1/4W	01121	CB 6805
A1R28	0683-6805		R:FXD COMP 68 OHM 5% 1/4W	01121	CB 6805
A1R29	0683-2715	2	R:FXD COMP 270 OHM 5% 1/4W	01121	CB 2715
A1R30	0683-2715		R:FXD COMP 270 OHM 5% 1/4W	01121	CB 2715
A1R31	0683-5105	2	R:FXD COMP 51 OHM 5% 1/4W	01121	CB 5105
A1R32	0683-5115	2	R:FXD COMP 510 OHM 5% 1/4W	01121	CB 5115
A1R33	0683-5115		R:FXD COMP 510 OHM 5% 1/4W	01121	CB 5115
A1R34	0683-5105		R:FXD COMP 51 OHM 5% 1/4W	01121	CB 5105
A1R35	0683-4715	2	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715
A1R36	0683-1025		R:FXD COMP 1000 OHM 5% 1/4W	01121	CB 1025
A1R37	0683-4715	3	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715
A1R38	0683-1025		R:FXD COMP 1000 OHM 5% 1/4W	01121	CB 1025
A1R39	0683-2425	1	R:FXD COMP 2400 OHM 5% 1/4W FACTORY SELECT	01121	CB 2425
A1R40	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R41	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R42	0683-2435	1	R:FXD COMP 24K OHM 5% 1/4W	01121	CB 2435
A1R43	0683-1055		R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A1R44	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R45	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R46	0683-3025	3	R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A1R47	0683-1045		R:FXD COMP 100K OHMS 5% 1/4W	01121	CB 1045
A1R48 PART OF A1R60 E1, E2	1801-0041		R:FXD 2.7K PART OF E1, E2	28480	1801-0041
A1R51	0683-1025		R:FXD COMP 1000 OHM 5% 1/4W	01121	CB 1025
A1R62	0683-3025		R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A1R63	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R64	0683-1035	3	R:FXD COMP 10K OHM 5% 1/4W	01121	CB 1035
A1R65	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R66	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R67	0683-5125		R:FXD COMP 5100 OHM 5% 1/4W	01121	CB 5125
A1R68	0683-1035		R:FXD COMP 10K OHM 5% 1/4W	01121	CB 1035
A1R69	0683-1035		R:FXD COMP 10K OHM 5% 1/4W	01121	CB 1035
A1R70	0683-3025		R:FXD COMP 3000 OHM 5% 1/4W	01121	CB 3025
A1U1	1820-0441	1	IC:DUAL 5-INPUT NAND GATE	04713	SC8171PK
A1U2	1820-0094	2	IC:DTL QUAD 2-INPT GATE	28480	1820-0094
A1U3	1820-0069	1	IC:TTL DUAL 4-INPT POS NAND GATE	01295	SN4344
A1U4	1820-0077	4	IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U5	1820-0273	2	IC:DTL QUAD 2-INPT AND GATE	28480	1820-0273
A1U6	1820-0094		IC:DTL QUAD 2-INPT GATE	28480	1820-0094
A1U7	1820-0077		IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U8	1820-0077		IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U9	1820-0068	2	IC:TTL TRIPLE 3-INPUT POS NAND GATE	12040	SN7410N
A1U10	1820-0307	1	IC:DIGITAL DTL HEX INVERTER	28480	1820-0307
A1U11	1820-0273		IC:DTL QUAD 2-INPT AND GATE	28480	1820-0273
A1U12	1820-0370	1	IC:TTL QUAD 2-INPT NAND GATE	01295	SN4478
A1U13	1820-0174	2	INTEGRATED CIRCUIT:TTL HEX INVERTER	01295	SN8199
A1U14	1820-0054	2	IC:TTL QUAD 2-INPUT NAND GATE	01295	SN4342
A1U15	1820-0077		IC:TTL DUAL D FF (LATCH)	01295	SN4354
A1U16	1820-0068		IC:TTL TRIPLE 3-INPUT POS NAND GATE	12040	SN7410N
A1U17	1820-0174		INTEGRATED CIRCUIT:TTL HEX INVERTER	01295	SN8199
A1U18	1820-0054		IC:TTL QUAD 2-INPUT NAND GATE	01295	SN4342
A1U19	1820-0511	1	IC:TTL QUAD 2-INPT & GATE	01295	SN20572
A1U20	1820-0328	1	IC:TTL QUAD 2-INPT NOR GATE	01295	SN4467
A1U21	1820-0578	1	IC:DIGITAL DUAL 2-INPT OR/NOR GATE	04713	SC7383PK
A1U22	1820-0577	1	IC:DIGITAL TTL HEX INVERTER	01295	SN22729
A1U23	1820-0253	2	INTEGRATED CIRCUIT:DIGITAL ECL DUAL	04713	MC1035P
A1U24	1820-0253		INTEGRATED CIRCUIT:DIGITAL ECL DUAL	04713	MC1035P
A2	05304-60002	1	BOARD ASSY:ATTENUATOR	28480	05304-60002
A2XA Misc.	05300-20007	1	PIN:CONNECTOR GROUP PC. Contains 36 pc right angle CONNECTORS. Only 14 are used.	28480	05300-20007
A2C1	0160-2250	2	C:FXD CER 5.1 PF 500VDCW	72982	301-000-C0H0-519E
A2C2	0160-2250		C:FXD CER 5.1 PF 500VDCW	72982	301-000-C0H0-519E
A2C3	0140-0208	2	C:FXD MICA 680 PF 5%	72136	RDM15F681J3C
A2C4	0140-0208		C:FXD MICA 680 PF 5%	72136	RDM15F681J3C
A2C5	0160-2199	2	C:FXD MICA 30 PF 5% 300VDCW	28480	0160-2199
A2C6	0160-2199		C:FXD MICA 30 PF 5% 300VDCW	28480	0160-2199
A2C7	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z
A2C8	0150-0075		C:FXD CER 4700 PF +100-20% 500VDCW	72982	851-000-X5U0-472Z

See introduction to this section for ordering information

Table 9D-7-4. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2J1	1250-1163	2	CONNECTOR:RF BNC INPUT	28480	1250-1163
A2J2	1250-1163		CONNECTOR:RF BNC INPUT	28480	1250-1163
A2R1	0683-9145	2	R:FXD COMP 910K OHM 5% 1/4W	01121	CB 9145
A2R2	0683-9145		R:FXD COMP 910K OHM 5% 1/4W	01121	CB 9145
A2R3	0683-9125	2	R:FXD COMP 9100 OHM 5% 1/4W	01121	CB 9125
A2R4	0683-9125		R:FXD COMP 9100 OHM 5% 1/4W	01121	CB 9125
A2R5	0698-3576	2	R:FXD COMP 110K OHM 5% 1/4W	28480	0698-3576
A2R6	0698-3576		R:FXD COMP 110K OHM 5% 1/4W	28480	0698-3576
A2R7	0683-1055		R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A2R8	0683-1055		R:FXD COMP 1 MEGOHM 5% 1/4W	01121	CB 1055
A2R9	2100-2905	2	R:VAR CERMET 10K OHM 10% LIN	28480	2100-2905
A2R10	2100-2905		R:VAR CERMET 10K OHM 10% LIN	28480	2100-2905
A2S2	3101-1313		SWITCH:SLIDE DP3T 0.5A 125V AC/DC	79727	G128S-0004
A2S3	3101-1313		SWITCH:SLIDE DP3T 0.5A 125V AC/DC	79727	G128S-0004
A2S4	3101-1596	4	SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
A2S5	3101-1596		SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
A2S6	3101-1596		SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
A2S7	3101-1596		SWITCH:SLIDE DPDT 0.5A 125V AC/DC	28480	3101-1596
			CHASSIS PARTS		
J1	1250-0083	2	CONNECTOR:BNC	02660	31-221-1020
C1	0160-0182	1	C:FXD 47 pf, 5%, 300V	14655	
J2	1250-0083		CONNECTOR:BNC	02660	31-221-1020
R43	2100-3078	1	R:VAR COMP 1 MEGOHM 20% (PART OF S2)	28480	2100-3078
S1	3101-1159	1	SWITCH:PUSHBUTTON SPDT	82389	10S-1051
S2	3100-2922	1	SWITCH:ROTARY	28480	3100-2922
S3			(PART OF R43)		
W1	05304-60004	1	CABLE ASSY	28480	05304-60004
			MISCELLANEOUS PARTS		
	0370-1005	2	KNOB:JADE GREY	28480	0370-1005
	0370-1100	1	KNOB:JADE GREY	28480	0370-1100
	0370-2102	1	KNOB	28480	0370-2102
	05245-2016	1	COUPLER	28480	05245-2016
	05300-40003	4	SUPPORT:BOARD	28480	05300-40003
	05300-40004	4	GUIDE:SLIDE	28480	05300-40004
	05301-20005	1	STAND:TILT	28480	05301-20005
	05300-80004	1	COVER: PLASTIC DUST PROTECTION	28480	05300-80004
	05301-40001	2	FOOT	28480	05301-40001
	05304-00001	1	PANEL:FRONT	28480	05304-00001
	05304-00004	1	PANEL:REAR	28480	05304-00004
	0624-0208	8	SCREW: SELF TAP, CAD. PLATE, 6/32 x 1/2"	28480	0624-0208

See introduction to this section for ordering information

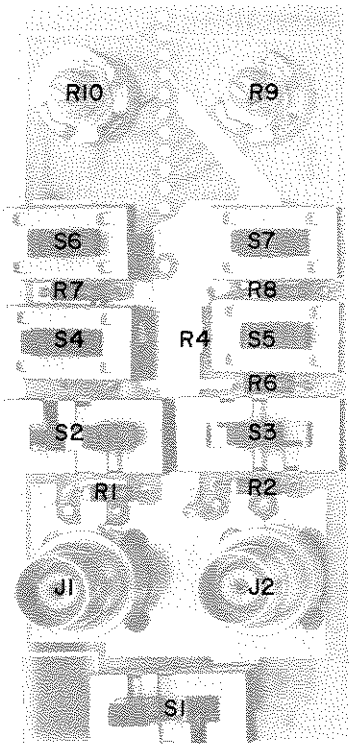


E1(3) — R60
E1(5) — R49
E1(6) — R50
E1(7) — R56
E1(8) — R58

E2(1) — R48
E2(2) — R54
E2(3) — R52
E2(4) — R59
E2(5) — R57

E2(6) — R55
E2(7) — R51
E2(8) — R53

A1



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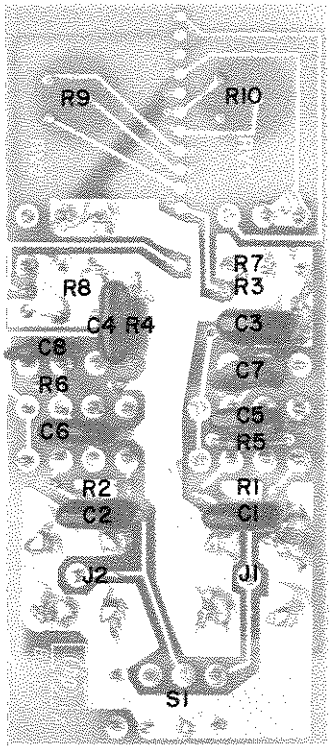


A2 Bottom

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS,
   CAPACITANCE IN PICOFARADS.

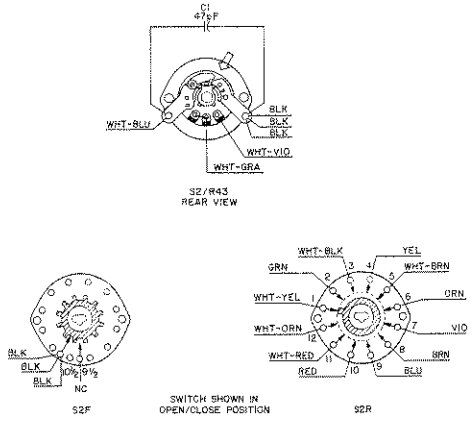
REFERENCE DESIGNATIONS

NO PREFIX	A1	A2
C1	C1-18 CR1-18 E1, 2	C1-8
J3, 4		J1, 2
	Q1-19	
R43	R1-70	R1-10
S1, 2		S1-7
	U1-24	

TABLE OF ACTIVE COMPONENTS

REFERENCE DESIGNATIONS	HP PART NUMBERS
CR1-4	1901-0376
CR5-12, 16, 17	1901-0040
CR13, 14	1902-0031
CR15	1902-3149
Q1-4	1855-0081
Q5, 9, 19	1853-0036
Q10	1854-0246
Q11, 12, 17, 18	1854-0094
Q13-16	1854-0071
U1	1820-0441
U2, 6	1820-0094
U3	1820-0069
U4, 7, 8, 15	1820-0077
U5, 11	1820-0273
U9, 16	1820-0068
U10	1820-0307
U12	1820-0370
U13, 17	1820-0174
U14, 18	1820-0054
U19	1820-0511
U20	1820-0328
U21	1820-0578
U22	1820-0577
U23, 24	1820-0253

5A364-5-1



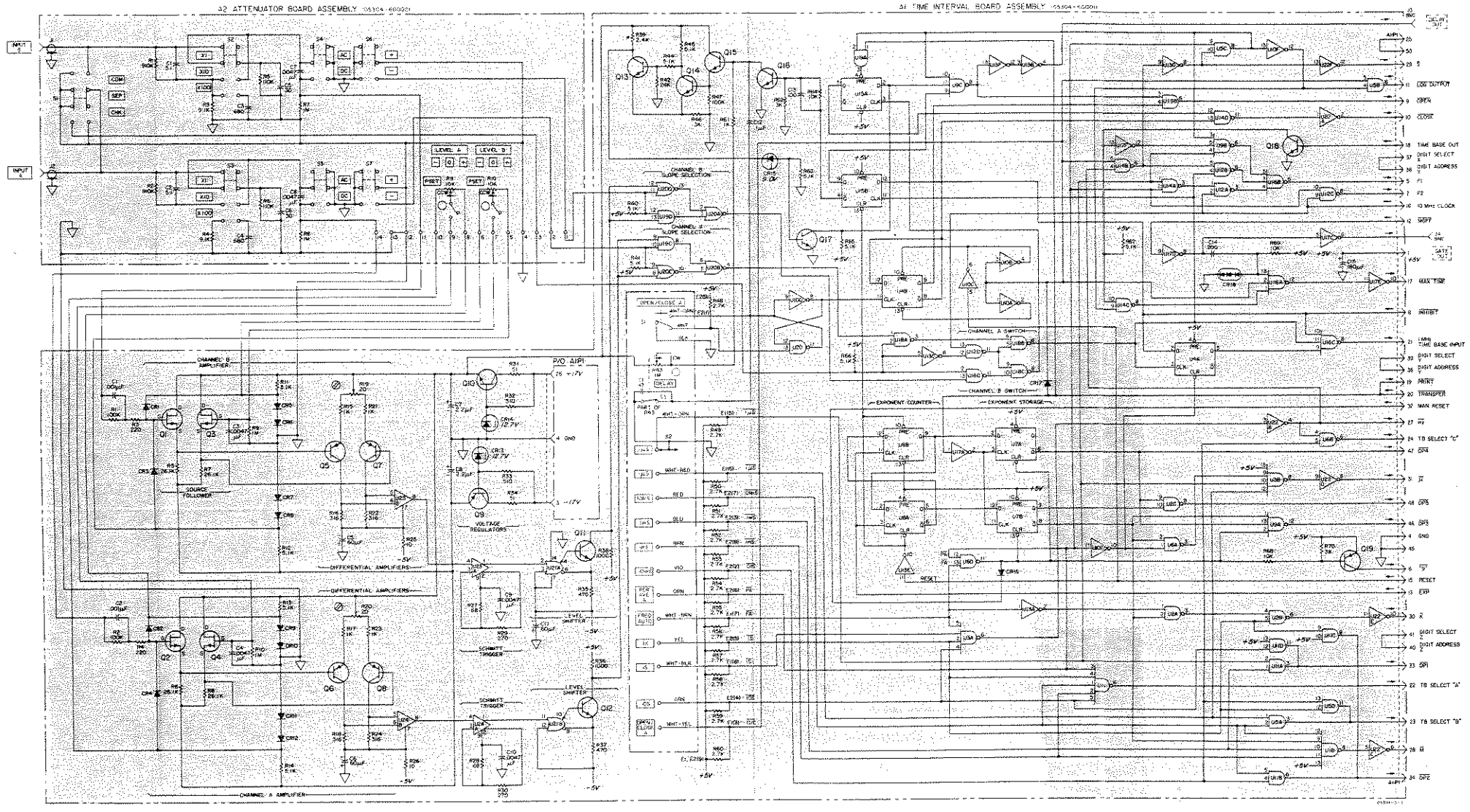


Figure 9D-7-1. A1 Time Interval Board Assembly
A2 Attenuator Board Assembly

SECTION IX D
5304A TIMER/COUNTER

SUBSECTION VIII
CIRCUIT DIAGRAMS

9D-8-1. GENERAL

9D-8-2. Subsection VIII contains:

a. Schematic diagram notes are contained in Section VIII of the 5300A portion of the manual.

b. Instrument interconnection pin list of signals listing where they originate and where the go.

c. Component locators, circuit and block diagrams of assemblies.

Table 9D-8-1. Instrument Interconnection List

PIN NO.	SIGNAL NAME	DESCRIPTION
1	+5 V	
2	-5 V	Input DC from 5300A
3	-17 V	
4	GROUND	
5 *	F1	This is the signal to be accumulated in the counter after gating by the control circuit.
6 *	$\overline{\text{"9"}}$	Goes low when the counter reaches 9% full scale.
7 *	F2	The input signal to the time base gated by the control circuit.
8	$\overline{\text{INHIBIT}}$	High during the measurement cycle, low during the display cycle.
9 *	$\overline{\text{OPEN}}$	Low signal forces the main gate flip-flop to the open position.
10 *	$\overline{\text{CLOSE}}$	Low signal forces the main gate flip-flop to the close position.
11	$\overline{\text{LOG}}$	Logarithmic output pulse train from time base triggers main gate flip-flop on rising edge.
12	$\overline{\text{MGFF}}$	Main gate flip-flop signal is low when gate is open.
13	$\overline{\text{EXPONENT}}$	Inverted log pulses while main gate is open indicates number of auto ranging steps.
14	NO CONNECTION	
15	RESET	High signal resets all registers.
16	CLOCK	10 MHz reference signal from crystal oscillator.
17 *	$\overline{\text{MAX TIME}}$	Low signal enables closing of the gate on next log pulse. Rising edge initiates display cycle.
18	TIME BASE OUTPUT	Output from the time base decade position selected by the time base select code on pins 22, 23, and 24.
19	$\overline{\text{PRINT}}$	Low signal provides print command to rear panel connector.
20	$\overline{\text{TRANSFER}}$	Low signal transfers data to display. High signal stores data.
21 *	1 MHz TIME BASE INPUT	Input direct from plug-on bypasses control circuit.
22 *	TIME BASE SELECT A	Time base select code A, B, and C selects the time base division factor of the signal at the time base output at pin 18.
23 *	TIME BASE SELECT B	
24 *	TIME BASE SELECT C	
25	+22 V	Full wave rectified voltage from the power transformer secondary. Provides power to charge the battery pack. If no battery pack is used, pin 25 is connected via the plug-on to pin 50.
50		
26	+17 V	
27 *	$\overline{\text{Hz}}$	
28 *	$\overline{\text{M}}$	Pins 27 through 31 provide the drive to the annunciator lights.
29 *	$\overline{\text{S}}$	on the front panel. A low signal lights the corresponding indicator.
30 *	$\overline{\text{K}}$	
31 *	$\overline{\mu}$	
32	$\overline{\text{MANUAL RESET}}$	Low signal from front panel pushbutton switch on rear panel input clears the system to zero.
33 *	$\overline{\text{DP1}}$	Low signal activates decimal point 1.
34 *	$\overline{\text{DP2}}$	Low signal activates decimal point 2.

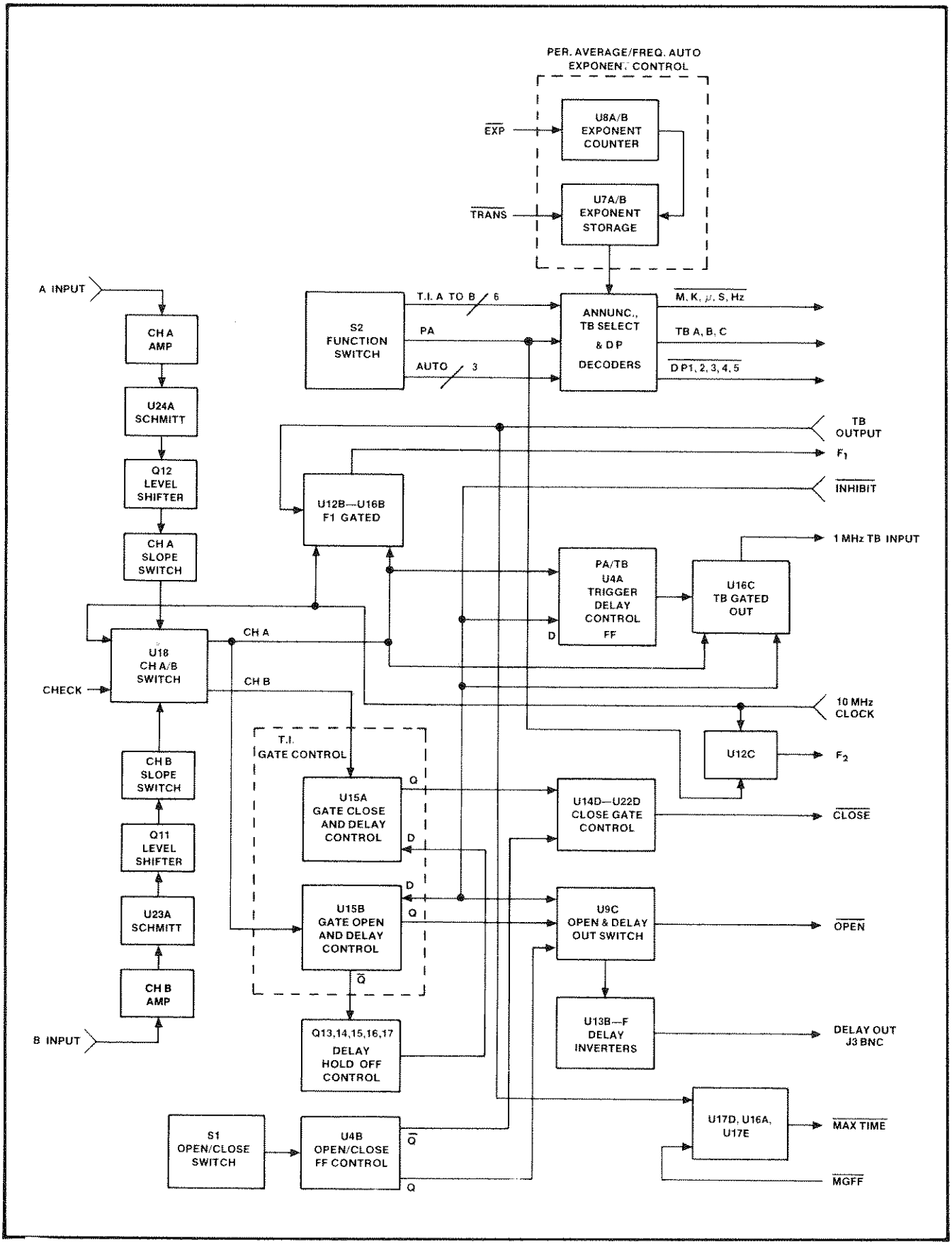
* = Source

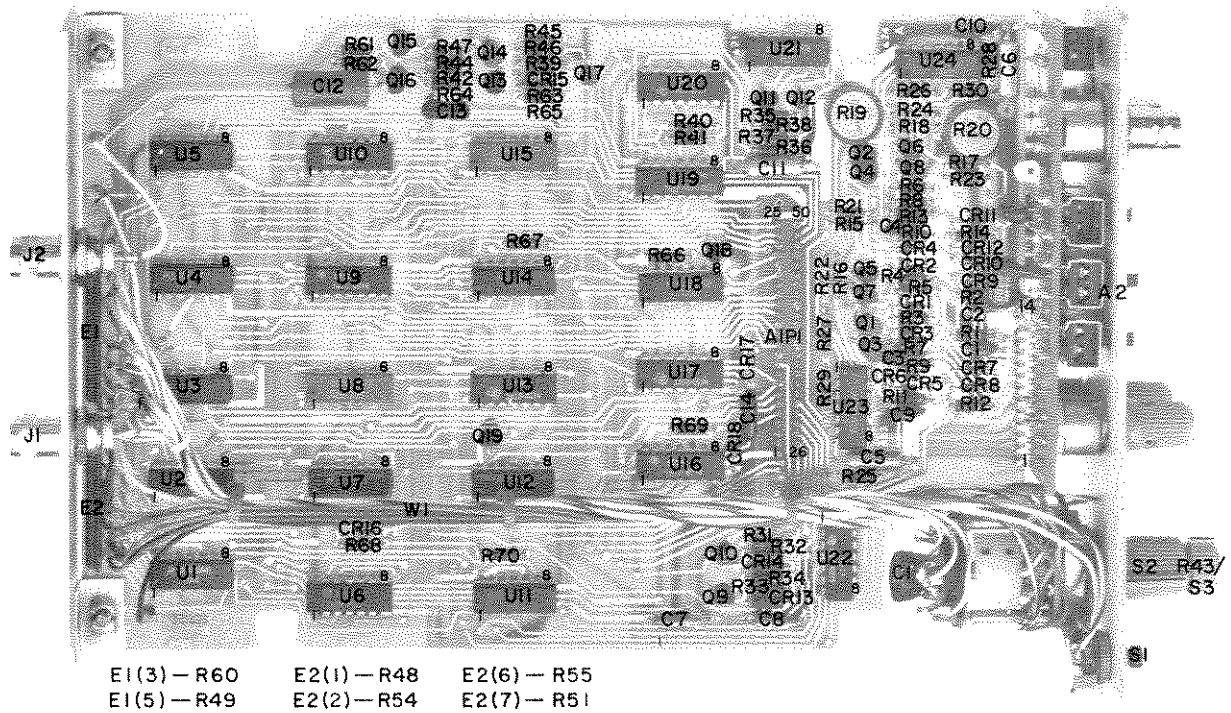
Table 9D-8-1. Instrument Interconnection List

PIN NO.	SIGNAL NAME	DESCRIPTION
35	NO CONNECTION	
36	DIGIT ADDRESS X	
37	DIGIT SELECT X	Digit address code X, Y, Z from the display scanner indicates a digit being displayed.
38	DIGIT ADDRESS Y	
39	DIGIT SELECT Y	DIGIT select code X, Y, Z is the corresponding code which selectes the digit at the output of the counter. If the main frame counter is displayed directly the corresponding lines of the digit address code and the digit select code are connected together.
40	DIGIT ADDRESS Z	
41	DIGIT SELECT Z	
42	NO CONNECTION	
43	NO CONNECTION	
44	NO CONNECTION	
44	NO CONNECTION	
45	NO CONNECTION	
46 *	$\overline{DP3}$	Low signal activates decimal point 3.
47 *	$\overline{DP4}$	Low signal activates decimal point 4
48 *	$\overline{DP5}$	Low signal activates decimal point 5.
49	NO CONNECTION	
50	DC IN	DC power to power supply from battery pack or from 22 volt input power from pin 25.
25		

*= Source

Part of Figure 9D-8-1. 5304A Block Diagram





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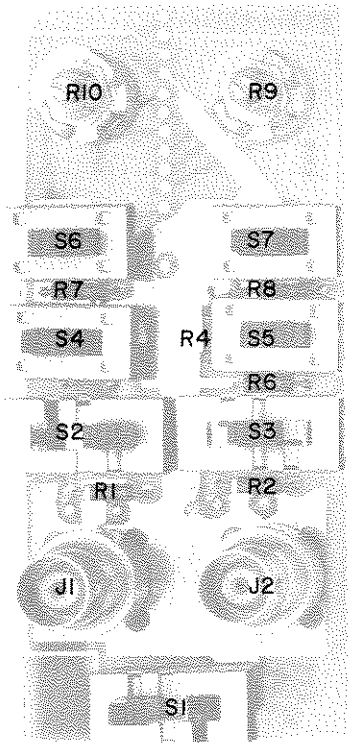

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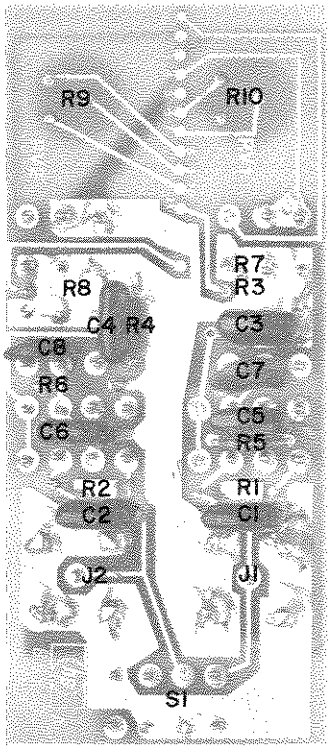

A2 Bottom

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	E1, 2	
J3, 4		J1, 2
	Q1-19	
R43	R1-70	R1-16
S1, 2		S1-7
	U1-24	

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Q11, 12, 17, 18	1854-0094
Q13-16	1854-0071
U1	1820-0441
U2, 6	1820-0094
U3	1820-0068
U4, 7, 8, 15	1820-0077
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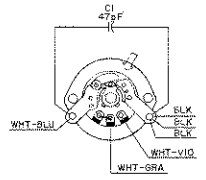
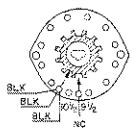
U12	1820-0370
U13, 17	1820-0174
U14, 18	1820-0054
U19	1820-0511
U20	1820-0338
U21	1820-0578
U22	1820-0577
U23, 24	1820-0253

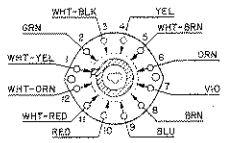
5304-8-1



S2/R43
REAR VIEW



S2F



SWITCH SHOWN IN OPEN/CLOSE POSITION

S2R

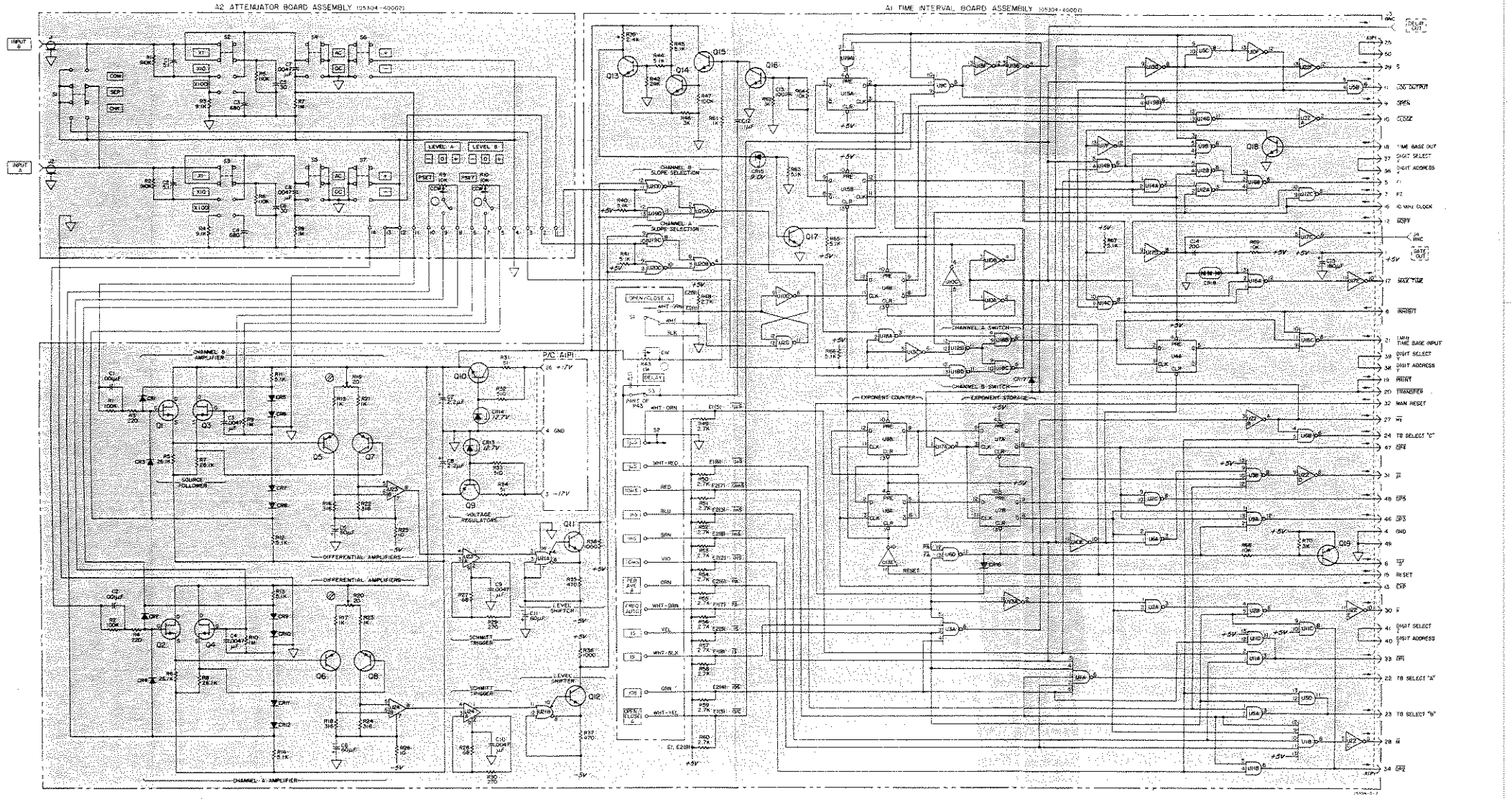


Figure 9D-8-1. A1 Time Interval Board Assembly
A2 Attenuator Board Assembly